PIC MAGAZINE

CONNECTING THE PHOTONIC INTEGRATED CIRCUITS COMMUNITY

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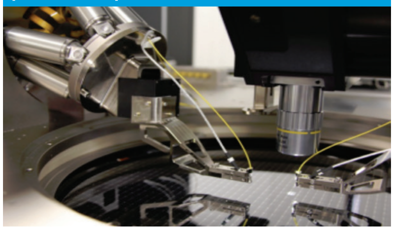
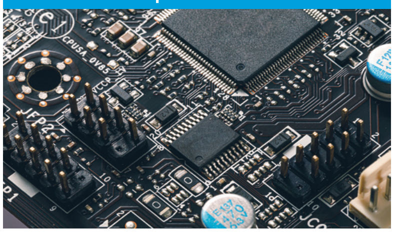
Practical examples of parallel photonics



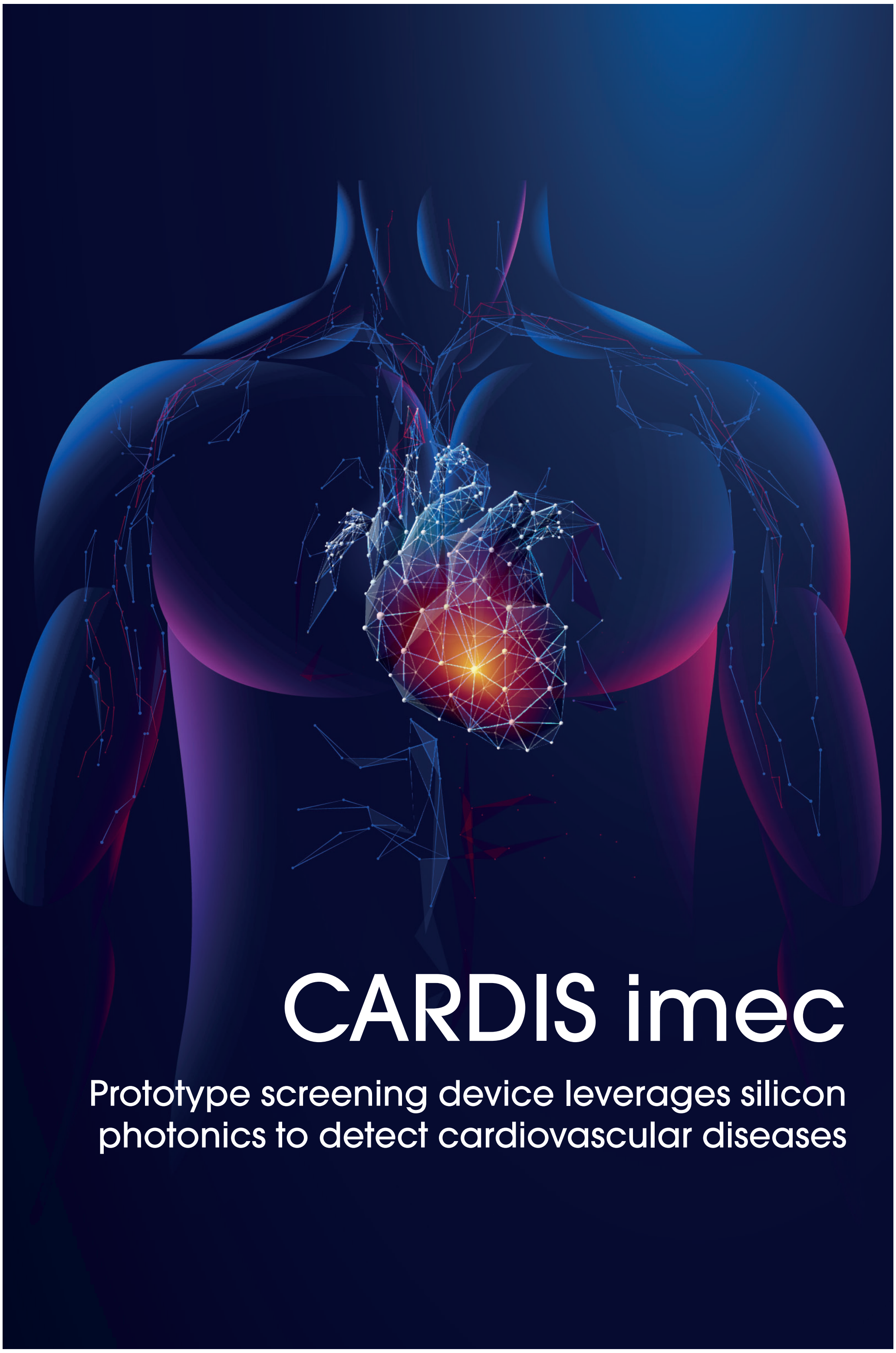
Integrated Poly-Si LEDs as on-chip micro biosensors

Fascinating ways digital olfaction is being used

Shining new light on moving data on chip



Valens unveils high-speed automotive chipset



Viewpoint

By Mark Andrews, Technical Editor

Opportunities, challenges will highlight ECOC 2019 in Dublin

THE PHOTONICS COMMUNITY will converge in Dublin 22-26 September for ECOC 2019. The conference's Market Focus programme is loaded with sessions addressing optical communications opportunities and challenges. As Europe grows as a photonics center of excellence, PICs and Silicon Photonics (SiP) will play an increasingly central role in the transition from pluggable to co-packaged transceivers along with innovative, post-400G product solutions. Photonic integration is also enabling advances in transportation, sensing and 5G networks.

While the ECOC programme dedicates a half-day to emerging technologies, looking closely reveals much more. Photonic integration, packaging and an ever-growing range of applications beyond telecom/datacom will highlight ECOC because these technologies are helping drive a photonics future by enabling faster, more efficient data communications, new and more accurate sensors, LiDAR systems critical to autonomous vehicles (AV), 5G networking, 3D facial recognition and the IoT.

Co-packaging along with automated test, assembly and packaging (TAP) is seen by most across the photonics ecosystem as a 'gate' through which PIC and SiP designers, developers and manufacturers all must pass to achieve profitability. A significant part of the growth potential projected for SiP/PICs hinges on miniaturized, high-performance optical devices entering markets with high volume potential. But there's a catch: for PICs to achieve their potential they must grow beyond the quality performance issues so common with first generation 100 Gbps transceivers. PIC and SiP device manufacturing must also standardize while implementing QC-methodologies based upon the principles that already serve other areas of the optics/photonics/electronics supply chain.

This edition of PIC Magazine includes an article from Physik Instrumente. PI is continuing to expand its TAP portfolio to address challenging PIC and SiP requirements by automating processes that today are often done manually, which can lead to quality excursions. We also have an article from CEA-Leti that points to some of the challenges that remain in the quest to perfect SiP processes and techniques.

Fraunhofer HHI explores an expanded role in photonics for Indium Phosphide (InP) MZMs, which became widely associated with long-reach telecom applications decades ago. According to Fraunhofer HHI experts, new InP modulators are ideal for metro and other short-reach applications.

We also look at the successful EC-funded CARDIS programme that developed a PIC-based, easy-to-use handheld device to detect cardiovascular disease (CVD). The technology is entering its second clinical trial in Paris and is expected to go into limited production once regulators are satisfied with its efficacy.

We look forward to seeing the global photonics community at ECOC in Dublin!

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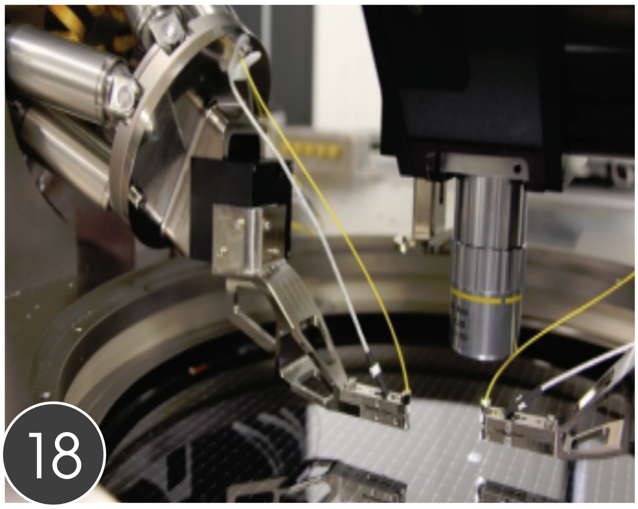
CONTENTS



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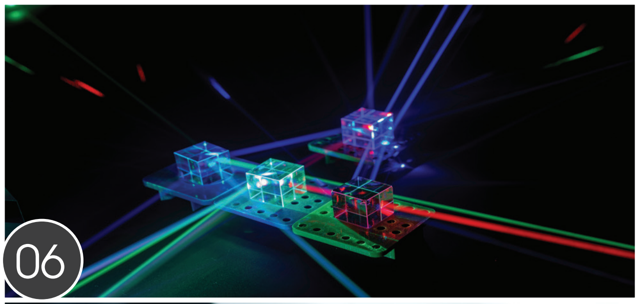
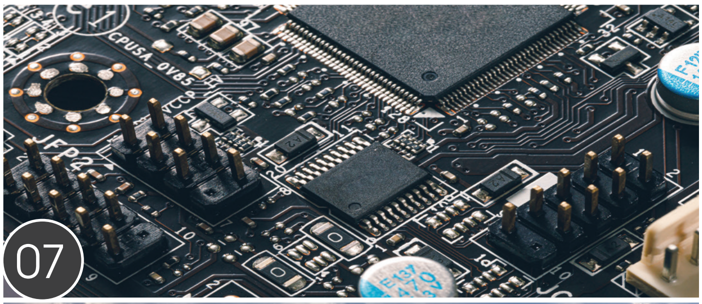




NeoPhotonics 30-40 mW CW laser sources

NEOPHOTONICS, a designer and manufacturer of advanced hybrid photonic integrated circuit based modules and subsystems for bandwidth-intensive, high speed communications networks, has announced general availability (GA) of its non-hermetic 30-40 mW DFB laser sources for use in Silicon Photonics 100G per wavelength CWDM4 FR4 and 1310 nm DR1 and DR4 transceivers. These lasers are available with and without integral Spot Size Converters (SSC).

NeoPhotonics low-loss SSC technology enables direct attachment of the Indium Phosphide laser to a Silicon Photonics waveguide, increasing manufacturing scalability and reducing costs. These efficient, high power DFB lasers can operate at up to 75 degrees C and are compliant with Telcordia GR-468-CORE, making them well suited for use in non-hermetic Silicon Photonics based small form factor pluggable modules, such as 400G QSFP-DD.

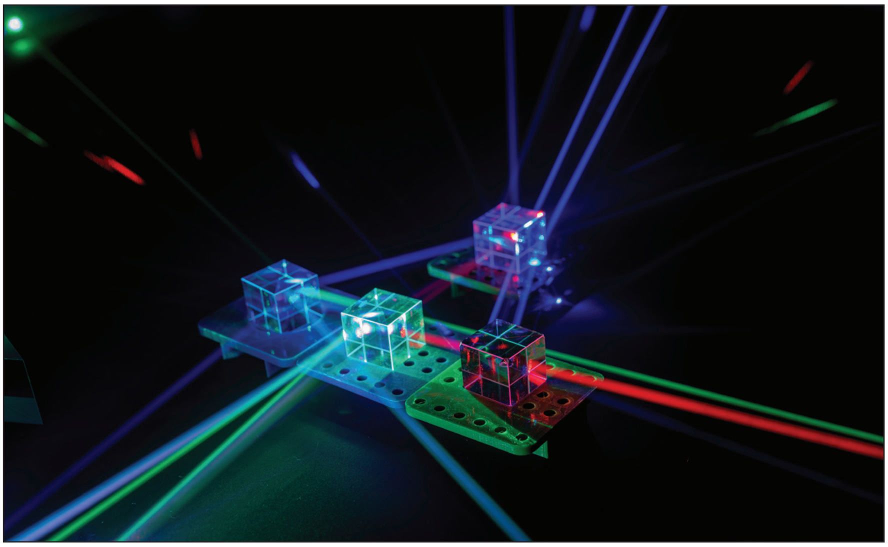
Silicon Photonics (SiPho) has emerged as a promising technology for optical data transmission over intermediate reaches of approximately 500 meters (DR) to 2 kilometers (FR) inside datacenters. A Silicon Photonics photonic integrated circuit can combine four different high speed modulators on a single chip, but it requires a light source to be modulated. A separate laser, or laser array, generating sufficient optical power at the specified wavelength(s) to overcome losses in the Silicon modulator and waveguides, must be coupled to the SiPho chip.

NeoPhotonics family of high power DFB lasers are designed to efficiently couple to the SiPho modulator chip and do not require hermetic packaging making them an ideal choice for next generation transceiver modules.

A high-speed SiPho modulator chip, due to its high VPi, generally requires a driver amplifier with a large voltage swing, which is also supplied by NeoPhotonics. NeoPhotonics Gallium Arsenide based Quad Driver chip combines four separate drivers in a single compact, low power chip designed to support compact pluggable modules such as OSFP and QSFP-DD.

"We are pleased to announce GA of our family of high power DFB lasers for next generation SiPho based 100G to 400G transceivers," said Tim Jenks, Chairman and CEO of NeoPhotonics.

"Silicon Photonics is rapidly transforming the data center transceiver marketplace by bringing the scale and cost structure of semiconductor electronics to optics, and our laser sources and drivers are helping to unleash the potential of Silicon Photonics," concluded Mr. Jenks.



PI's alignment technology at ECOC

DELEGATES at this year's European Conference on Optical Communication (ECOC 2019) – from the 23 - 25 September in Dublin – can see how Physik Instrumente's cost-effective and space saving technologies and solutions are improving accuracy and productivity for manufacturers in the photonics industry.

PI has been developing and manufacturing products that demand exceptional precision across a broad dynamic range for over 40 years, and visitors to Stand #357 can discover how the company's ground-breaking Fast Multi-Channel Photonics Alignment (FMPA) technology is revolutionising the probing, testing and packaging of silicon photonic devices. FMPA can simultaneously align multiple couplings and channels, across multiple degrees of freedom, even if they interact.

It offers much higher speed and accuracy than traditional methods, reducing alignment times from hours down to a few seconds. This innovative solution is already significantly reducing operating costs and improving overall efficiency and scalability around the world, without compromising on device quality.

Attendees also can see the F¬712.HA2 High-Precision Double-Sided Fibre Alignment System in action – an example of a double-sided system that allows simultaneous alignment of transmitters and receivers – as well as other outstanding alignment solutions for the photonics industry.

EFFECT Photonics receives investment from PhotonDelta

EFFECT Photonics, a developer of high performance dense wavelength division multiplexing (DWDM) optical components based on its optical System-on-Chip technology, today announced an investment from PhotonDelta.

EFFECT Photonics has secured €5M in funding to support its growing 5G and data centre business. The funds will be used to further accelerate product development and business scale-up, and thereby strengthens the integrated photonics ecosystem.

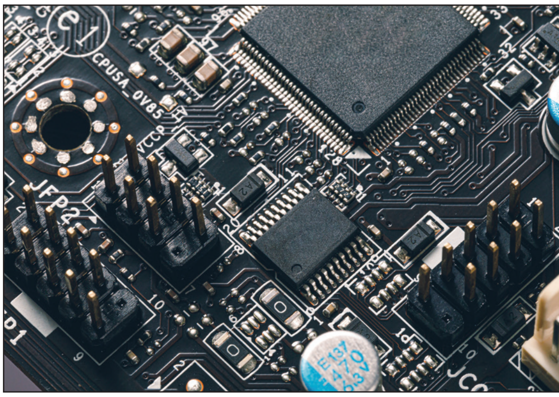
EFFECT Photonics' CEO James Regan says the Internet of Things, virtual reality, and cloud services are growing in popularity every day, increasing the demand for the best service possible. "These applications all depend on the next generation of connectivity, and 5G mobile infrastructure relies on the backing of a world-class optical network enabled by EFFECT Photonics. We are extremely proud that PhotonDelta shows this confidence in us, and are certain that the investment will support our ongoing work to enable this next era of photonics connectivity."

CTO Boudewijn Docter adds: "At EFFECT Photonics, we integrate all of the optical functions into a single chip and combine it with low-cost, non-hermetic packaging and automatic tuning. Thus DWDM – the proven solution for core and metro networks – is now simple, cost-effective and scalable enough for 5G infrastructure rollouts around the world. This funding allows us to really push forward our nextgeneration products to bring even more powerful optical systems to the edges of the network".

PhotonDelta CEO Ewit Roos explains: "EFFECT Photonics is a key player within our ecosystem, a frontrunner that develops and delivers complex integrated optical products in a high-volume global market that demands 5G connectivity now. To this end, we are thrilled to fund EFFECT Photonics in developing their products and scaling up their business.

Their products are supported by many other companies in the field of photonic integration services and components. Thus, the business growth of EFFECT Photonics has a profound impact as it leverages the scale of activity and innovation of the entire supply chain of integrated photonics in the Netherlands."

Shining new light on moving data on chip



A UNIVERSITY OF TEXAS at Dallas researcher has received an award from the US Department of Defense's Army Research Office Young Investigator Program to develop a nanoLED technology to be used in integrated circuits. The award provides Qing Gu, assistant professor of electrical and computer engineering, more than $356,000 over three years to support work to create an on-chip light source to carry data.

During her doctoral research, Gu created a nanolaser that could be used as a light source in on-chip optical communication systems. Now, however, she believes that nanoLEDs -- or tiny light-emitting diodes -- have the potential to perform better than nanolasers.

In addition to examining nanoLEDs, Gu's project includes designing and testing the infrastructure to make the light source and integrated circuit efficient.
"We want to look at not only the device itself but also the driver circuitry, and comprehensively evaluate the entire optical interconnect," Gu said. "We are not only doing device-level work, but we are also looking at the system-level performance. Our goal is to show that nanoLEDs are a better candidate than nanolasers for chip-scale data transportation." The potential to allow for faster and more efficient data transmission has a range of military applications.

"This cutting-edge work with nanoLEDs could have a broad impact on the Army," said Mike Gerhold, program manager for electronics at the Army Research Office, an element of the US Army Combat Capabilities Development Command. "This research could lead to the development of low-energy data communications for faster and more energy-efficient electronic systems. Other applications would include active electro-optical systems where optical beam steering and sensing is needed."

Lawrence Overzet, head of the Department of Electrical and Computer Engineering at UT Dallas, said Gu's research has far-reaching implications. "When your internet company tells you that it is bringing an optical fibrd to your home, you know that your internet speeds will increase by a factor of 10, 100 or even a thousandfold. This is at the large scale, but Dr. Gu's research is looking to bring the increased data speeds down to the chip level, too -- the micro- and nanoscale," Overzet said. "This is both much more difficult and much more exciting. Dr. Gu's research is at the cutting edge of photonics, and we are excited about what she brings to electrical and computer engineering at UT Dallas."

The Young Investigator Program is designed to identify and support scientists and engineers who show promise for doing creative research in order to encourage their teaching and research careers.

Valens unveils high-speed automotive chipset

VALENS has unveiled its latest automotive chipset - the VA608A. The chipset delivers data transmission speeds of up to 16Gbps and enables automakers to extend native PCIe as a long-distance in-vehicle connectivity technology - up to 15m/50ft. The VA608A is also the first and only chipset to enable 2.5Gb Ethernet over a single Unshielded Twisted Pair (UTP) wire with near-zero latency.

With the VA608A, Valens is introducing an innovative concept for long-distance PCIe connectivity, enabling OEMs and Tier-1s to utilize a wide array of existing components without requiring a complete redesign of the vehicle's architecture. This leads to reduced costs and wiring complexity, and the ability to utilize more powerful technologies with increased speed and functionality. Valens' PCIe extension technology is designed for many use cases in the vehicle including telematics, multi-modem smart antennas (5G, WiFi, WiGig, BT, etc.), ECU-to-ECU connectivity, and shared storage/black box storage. It also significantly simplifies high-speed, low latency, power-efficient backbone architecture.

"The VA608A is a game-changing chipset technology for the automotive industry," said Daniel Adler, Vice President & Head of Automotive Business Unit, Valens. "Valens continues to lead the way with unprecedented ultra-high-speed, multi-Gigabit in-vehicle connectivity solutions, introducing innovative concepts and approaches for smarter vehicle architectures. From the outset, our goal has been to provide the most resilient solution for connectivity applications while reducing overall system costs, both in terms of infrastructure and software components. The VA608A fulfils that goal."

Valens' technology is a scalable solution specifically designed to handle harsh EMI and environmental interference in the vehicle landscape. The VA608A is an ASIC prototype and is currently available.

The VA608A launch comes on the heels of the MIPI Alliance's selection of Valens' technology as the baseline for its A-PHY standard for ultra-high-speed in-vehicle video transmission. MIPI's A-PHY specification defines an asymmetric physical layer for the automotive market to provide high-speed links for cameras, displays and sensors, through native CSI-2 and DSI/DSI-2 interfaces, addressing autonomous applications. Following an in-depth evaluation process, including testing and analysis of several proposed solutions from MIPI's member companies, Valens' solution was determined best-suited to address the need for high-speed, in-vehicle video links, and to support the range of bandwidth defined by MIPI's automotive standard, as published by the MIPI Alliance.

The final specification is expected to be completed by the end of 2019. MIPI's will be the first high-speed asymmetric standard in the market.

CompoundTek and Luceda release a PDK

COMPOUNDTEK, a global foundry services leader in emerging silicon photonic (SiPh) solutions recently partnered with Luceda Photonics, a leader in integrated photonics design automation. Together they will expand CompoundTek's silicon photonics Process Design Kit (PDK) offering to enable Luceda's IPKISS platform for a global commercial customer base.

Photonic IC technology is maturing fast with designers needing PDKs as the foundation of their design flow. Providing a reliable and scalable design flow, the PDKs additionally facilitate knowledge transfer between foundries and designers on layout and simulation models. The IPKISS platform combines layout, smart physical simulation and circuit level design and simulation, in one single quality-controlled PDK. The PDK can be used from IPKISS.flow, and from IPKISS.eda integrated in the Siemens / Tanner flow, enabling customers to make significant strides forward in creating design flows that are more reliable and scalable.

Pivotal to the consolidation of knowledge in the context of a fast-moving industry, the IPKISS platform is instrumental to producing a scripting environment that covers the complete photonic IC design flow up to measurement feedback for true component validation. This is suited for niche solutions spanning interconnectivity, datacom transceivers, bio-sensing, smart sensors, LiDAR, quantum computing, and artificial intelligence. "Our strategic partnership with Luceda Photonics leverages CompoundTek's open manufacturing process platform. Backed by an ecosystem that includes our design partners and foundry, the photonics design automation solution will further accelerate time-to-market in cutting-edge SiPh solutions," said KS Ang, Chief Operating Officer, CompoundTek.

"The PDK with CompoundTek has been created following demand of some of our most important customers. In adding an influential foundry to our portfolio, we open new design opportunities to mature yet innovative design teams," added Pieter Dumon, Chief Technology Officer, Luceda Photonics.

Infinera enhances Australian broadband network

INFINERA has announced that NBN Co, Australia's wholesale open-access broadband provider, has installed self-healing capabilities into its transit network with the deployment of Infinera's Transcend software-defined networking (SDN) solution. Infinera's SDN-based dynamic service rerouting capabilities for dense wavelength-division multiplexing (DWDM)-based networks allow network operators to restore customer services by automatically rerouting traffic when faults occur.

For NBN Co, the solution will be deployed across its 60,000-kilometer fibre optic transit network. NBN Co's transit network is a backbone network of fibre optic cables that links hubs across Australia to the wider nbn broadband access network that connects homes and businesses. This network moves large aggregate volumes of data between locations, delivering capacity to homes and businesses.

The network connects to NBN Co's 121 points of interconnection (POIs) – typically located at telephone exchanges – which are where phone and internet providers plug their own networks into the NBN Co access network.

The reconfigurable optical add-drop multiplexer (ROADM) technology enhancements introduced on the Infinera 7300 Series Multi-Haul Transport Platform will allow NBN Co to increase its network resiliency and reliability by introducing automatic service restoration capabilities across its transit network.

"The Transcend SDN solution was deployed and integrated with our systems, giving us the capability to increase service availability to some of the most remote locations across Australia," said NBN Co's chief network deployment officer, Kathrine Dyer. "This will give our network increased resiliency and help ensure that our customers get the best possible experience when migrating to NBN Co's broadband access network."

"We are delighted to work with NBN Co by providing innovative software and automation solutions that help them overcome the challenges of operating a large nationwide network," said Bob Jandro, senior VP, worldwide sales at Infinera. "Transcend's service restoration and management capabilities are ideal for network operators like NBN Co to

differentiate themselves in a competitive market by providing the most reliable services."

NBN Co's network enhancements are based on Infinera's 7300 multi-haul DWDM platform with Infinera's Transcend SDN solution spanning several transport layer technologies – such as optical DWDM layers and electrical Optical Data Unit (ODU) switching layers – to provide end-to-end service control and enable SDN-based service control for Infinera's optical and packet-optical transport portfolio.

It also offers open and standards-based RESTful northbound interfaces to provide real-time, programmable multi-layer control to higher-layer controllers and provides a foundation to introduce programmable networking and automation in the NBN Co environment.

Trymax receives order from photonics research organisation

TRYMAX Semiconductor Equipment BV (Trymax), a supplier of plasma solutions, has announced it has received an order from NanoLab@TU/e of Eindhoven University of Technology.

The NEO 200A series from Trymax with microwave downstream plasma technology was selected to perform resist stripping, descum and surface cleaning on indium phosphide (InP) wafers. This order illustrates the competitiveness of the single chamber and fully automated solution of Trymax for the photonics market.

"European research organizations and equipment companies are at the forefront of the global photonics industry" commented Carlos Lee, Director General of European Photonics Industry Consortium (EPIC). "Having a company such as Trymax collaborating with Eindhoven University of Technology goes in the right direction to build an efficient manufacturing infrastructure".

Eindhoven University of Technology selected Trymax after running technical demonstrations on InP substrate and other compound semiconductor substrates.

The results achieved on the NEO 200A platform in term of ash rate, non-uniformity and handling of critical substrate materials of different sizes outperformed competing solutions. "Beyond silicon, Trymax has a long experience and unique capabilities in handling various substrates materials such as SiC, GaN, GaAs, LiNbO3, LiTaO3, glass, and eWLB" stated Leo Meijer, CEO of Trymax.

"Having a recognized university such as Eindhoven University of Technology as a customer is an honor. Trymax, as a Dutch headquartered company, is proud to have the researchers and students from Eindhoven University of Technology developing the photonic solutions of the future with our system".

"Eindhoven University of Technology has chosen the Trymax NEO 200A because of the robustness of the tool, the expertise of the Trymax team and the short distance to the lab, all which is superior to what we found elsewhere on the market" mentioned Huub Ambrosius, Managing Director of NanoLab@TU/e.

The NEO 200A system will be installed at Eindhoven University of Technology in Q3 2019.

Prototype screening device leverages silicon photonics to detect cardiovascular diseases

The successful EU-funded CARDIS project created a better means to diagnose and treat one of humanity's greatest health threats: cardiovascular disease (CVD). The handheld prototypes, now in clinical trials, leverage advanced sensors to deliver results accurately while being faster and simpler than legacy tools. PIC Magazine invited Prof. Dr. Roel Baets, principal researcher and project coordinator, to speak about ways that CARDIS points to the future of healthcare.

By Roel Baets, Professor at Ghent University (Belgium) and associated with imec

EACH YEAR, cardiovascular diseases (CVDs) are responsible for 30% of deaths worldwide. Key to reducing their impact (i.e. to avoid hospitalization and reduce CVD morbidity and mortality rates) are tools and devices that help general practitioners and paramedical personnel diagnose CVDs in an early stage.

Current CVD risk assessment methods are largely based on clinical judgment and traditional vital signs measurements (heart and respiratory rate, blood pressure, etc.). More ideally, however, those vital sign measurements should be complemented with new biomarkers such as pulse wave velocity (PWV) to get to a more accurate diagnosis. Adding PWV data – an important biomarker for arterial stiffness – is regarded as a very important first step to improving diagnoses. However, no tools are available today to easily screen large numbers of patients' PWV at doctors' offices.

In this context, and within the scope of the recently finished European H2020 CARDIS project, researchers have developed a mobile (handheld) and low-cost point-of-care CVD screening device based on silicon photonics. This device measures a patient's pulse wave velocity in a fast, reproducible and reliable way. A medical screening using the CARDIS device is non-invasive and requires minimal operator skills. Putting the prototype's capabilities and performance to the test, a clinical feasibility study with 100 patients has already successfully been completed at the Georges Pompidou European Hospital in Paris (France).

Challenging the gold standard to measure pulse wave velocity (PWV) in the arteries

Pulse wave velocity is defined as the velocity at which pressure waves, generated by the contraction of the heart, propagate along the arterial tree. It is an important marker for the stiffness of the arteries and can complement more traditional clinical parameters (e.g. blood pressure) to assess the risk of developing conditions such as atherosclerosis (with plaque – such as fat, cholesterol or calcium – building up inside one's arteries, over time hardening and narrowing those arteries) and arteriosclerosis (the thickening and hardening of the artery walls).

Today's gold standard to measure one's pulse wave velocity relies upon pressure sensors being placed over the carotid artery in the neck and the femoral artery in the groin to measure the speed with which pulse waves travel down the aorta. Such PWV measurements, however, come with quite some drawbacks: it is a pretty cumbersome approach and does not allow for a quick and easy screening of large numbers of patients. Moreover, it only provides the average PWV over a long segment of arteries (each having different mechanical characteristics) – meaning that it cannot be used to evaluate arterial stiffness in a small area; nor will it give information about the exact location of any arterial abnormalities.

Prototype medical device to perform LaserDoppler Vibrometry on a patient's skin to deduce metrics for arterial stiffness and to diagnose cardiovascular diseases

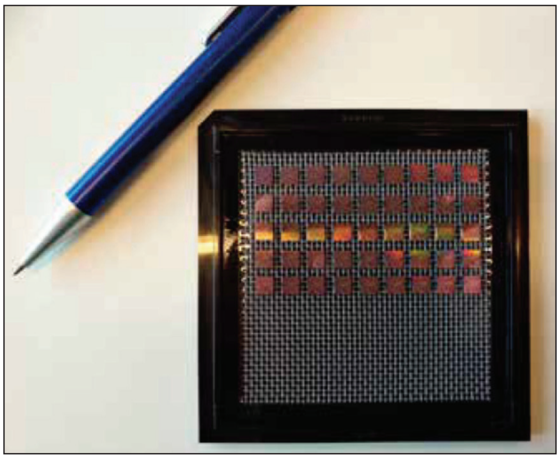
In response to those limitations, the prototype handheld device that has been developed and tested by the CARDIS consortium measures pulse wave velocity more locally – making for a quick and easily reproducible assessment, while still allowing for the carotid-femoral measurement.

Leveraging the compactness and cost-effectiveness of silicon photonics

The CARDIS prototype device makes use of multi-beam Laser Doppler Vibrometry (LDV), whereby a set of low-power laser beams are shone onto the skin above the carotid artery of the patient. The power level is so low (well below 1 mW) that it is completely harmless to the eye and skin. The reflected light is Doppler shifted in optical frequency due to the tiny movements of the skin above the artery as a result of the heartbeat. By doing measurements at multiple locations, the PWV can be deduced.

The new CARDIS device is very compact because it makes use of silicon photonics for the basic LDV engine, allowing the hardware to be miniaturized to a handheld device.

The photonic chips which are at the heart of the system have been designed and manufactured at imec using the silicon photonics iSiPP50G process – including passive functions, modulation and switch functions as well as germanium detectors. The chip is co-assembled with a micro-optic bench holding a 1550nm single mode laser, a miniature optical isolator and coupling structures to the chip. The packaging



The photonic chip, key in realising the handheld device for measuring arterial stiffness

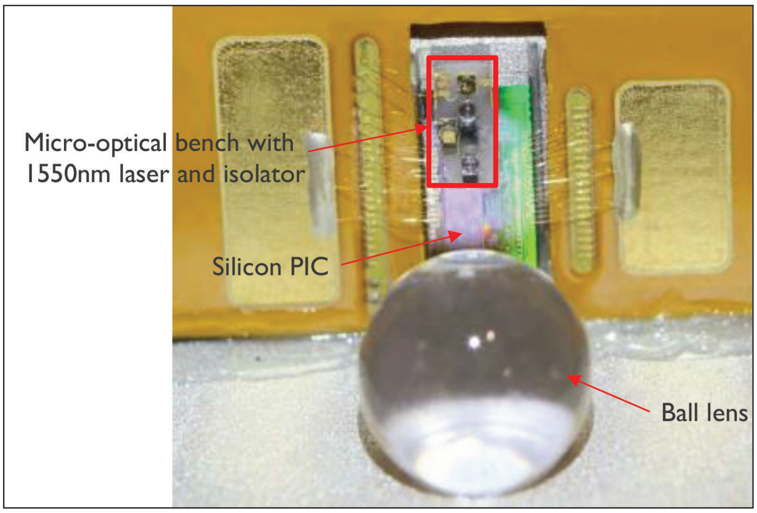
of the photonic chip was executed at Tyndall National Institute (Cork, Ireland).

Imec's integrated Silicon Photonics Platform co-integrates a wide variety of passive and active components, thus enabling competitive photonic integrated circuits for a broad range of functionalities and markets – including data centers, telecom, sensors, LIDAR, etc. As demonstrated in the CARDIS use-case, silicon photonics makes a huge difference when a device needs to be miniaturized to the extreme, or when the device – as in the case of a point-of-care device – needs to be optimized with respect to cost; but also when reliable manufacturing and/or large volume production is needed.

Putting the prototype to the test during a clinical feasibility study

The CARDIS prototype has been put to the test during a clinical feasibility study with 100 patients at the Georges Pompidou European Hospital in Paris, whereby a substantial clinical dataset has been collected – both from healthy subjects as well as from patients with cardiovascular conditions.

The quality of the device's readings was found to be very good and adequate measurement results could be obtained in all subjects. When using the device in a carotid-femoral mode, the measurement data as well as the variability within sessions were in line with those acquired by reference techniques. That being said, the local carotid measurement approach is substantially more demanding with respect to the algorithms to extract robust PWV-numbers – so further optimization is still needed.



Packaged silicon photonic chip with co-assembled laser source, optical isolator and ball lens for coupling light back and forth to the patient's skin.

According to the cardiologist in charge of the feasibility study, the CARDIS device was well accepted by all patients, and considered useful by the medical staff. The team noted that a useful signal was acquired in 100% of the patients. Tolerance was excellent too, the time to get useful signals was less than 10 minutes, and patients barely noticed that a measurement was performed.

Technological and medical next steps

The team's future plans are two-fold. At the technological level, they want to continue to improve and optimize the user-friendliness of the device – for instance by making it completely wireless and substantially lighter and smaller. At the medical level, the data provided by the CARDIS device will be validated more in-depth against other methods.

To this end, the algorithms used to convert the LDV signals in relevant and robust medical markers will be finetuned up to the point where they will allow for diagnostic and therapeutic decision-making.

In a next step, a small series of prototype devices will be produced to perform a clinical feasibility study on a larger group of patients over a longer period of time. If this feasibility study demonstrates the technology's ability to detect cardiovascular diseases at an early stage, high volume production can be initiated. Again, one of the benefits of the silicon photonics technology is that – at high volumes – the chip can be produced at low cost.

It is worth noting that Laser Doppler Vibrometry (LDV) can support a wealth of other applications beyond the medical case described here. It can be used for structural monitoring of critical infrastructure (e.g. bridges), to capture acoustic signals, and much more. For many of those applications, miniaturization and cost are key to their widespread introduction. As such, the future of LDV, enabled by silicon photonics, looks bright!

- **About CARDIS:** *The H2020 CARDIS project consortium includes a variety of partners – from widely acknowledged universities to leading technology companies: Ghent University, imec, INSERM, Maastricht University, Medtronic, QMUL, SIOS and Tyndall. The project was coordinated by Fundico.*

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Silicon photonics market growth depends on maturing processes and overcoming TAP challenges

Initial optimism over Silicon Photonics (SiP) potential to unseat incumbent transceiver and switch technologies suffers today from the years it took process tool and TAP manufacturers to adapt CMOS hardware to the eccentric needs of photonic device manufacturing. CEA-Leti experts delve into potential remedies that could be the tonic SiP needs to lead in short- and medium-reach applications.

By Daivid Fowler[a], Phillipe Grosse[a], Stéphane Bernabé[a], Fabien Gays[a], Bertrand Szelag[a], Charles Baudot[c], Nathalie Vuillet[b], Jonathan Planchot[b] and Frederic Boeuf[b] CEA-Leti, Grenoble, France[a], STMicroelectronics, Crolles, France[b], ACCIENA, Québec, Canada[c]

FOLLOWING the initial demonstrations of silicon-based photonic devices in the 1990s[1], the suggestion that photonic integrated circuits (PICs) could be cheaply and reliably mass-produced using existing CMOS infrastructure led to optimism that this technology could rapidly supplant established technologies for short-to-medium range digital communications[2]. Today, silicon-photonics based transceivers are gaining market share, especially for single-mode fibre-based interconnects in hyper-scale data-centres. Several companies like Intel and Cisco have significantly invested a lot of technology, putting 100 Gbps modules on the market while beginning to roll out 400 Gbps versions.

However, silicon photonics is still competing with VCSELs for short range (<300m) and with InP-based modules for Inter Data-Centre interconnects, resulting in fewer sales than expected a decade ago. This is despite the increasing number of Si-based photonic components and circuitry with demonstrated performance comparable to, or in excess of, equivalent discrete optical components. One of the reasons behind this delay may have been the initial time to develop a photonic-specific fabrication process, as well as the availability of key software and hardware for simulation, layout and test that must be heavily adapted with respect to standard CMOS electronics infrastructure.

At CEA-Leti, whose role is to develop emerging technologies for transfer to industry, our silicon photonics program has been working to this end with numerous academic and industrial partners (e.g. within the IRT Nanoelec program) since from about 2005.

Among the various components we have developed, the fibre grating coupler (FGC) illustrates this situation very well. This structure is used to couple light from the PIC to an optical fibre, and its performance in terms of insertion loss (IL) is a key specification for allowing Si-photonic transceivers to compete with other technologies. Indeed, one of the unique challenges to creating low-cost silicon-photonic transceivers is an efficient means to couple light from a single-mode fibre with a mode field diameter of ~10μm, to an on-chip mono-mode Si waveguide, which due to the large optical index contrast of Si/SiO_2 has a mode size of just several hundred nanometric. Indeed, this mode size mismatch is at the origin of a significant cost both monetarily and in terms of optical losses related to fibre coupling to Si-based PICs. Several solutions exist, but the use of diffraction-grating-based fibre couplers is well established due to the convenience of wafer-scale testing and relatively large alignment tolerances[3].

Figure 1 shows the general architecture of a recent version of the CEA-Leti O/C band fibre grating coupler [4]. It is composed of 310nm-thick SOI on a 1500nm BOX layer, partially etched to 160nm and fully encapsulated in SiO_2. Input guided light is diffracted by a series of pits, narrow and wide trenches towards an out-of-plane single mode fibre placed at 8° to the vertical. The non-uniform, curved diffraction grating is carefully optimised using Finite-Difference Time Domain (FDTD) simulation so that the output optical field best overlaps the Gaussian mode profile of the fibre, in order to decrease mode-matching losses. The minimum pit size is ~110nmx140nm and the minimum continuous trench width is 120nm. The fabrication process uses (non-immersion) 193nm lithography on 300mm wafers, with a CMOS equivalent node-size of 65nm.

Although the minimum feature size is significantly in excess of the notional minimum critical dimension of the lithography, this collection of non-rectilinear geometrical features of widely varying size, creates particular challenges for device fabrication with technology derived from CMOS electronics. Firstly, layout files entering a CMOS foundry environment undergo automatic 'Design Rule Checking' (DRC) to alert the designer to errors as well as to highlight design aspects that are not compatible with subsequent stages of fabrication. Until the recent emergence of DRC tools with 'equation-based' algorithms (e.g. Calibre nmDRC from Mentor Graphics), access to CMOS foundries has relied on the adaptation of DRC software designed for the 'Manhattan' layouts found in electronics. Owing to the wide variety of shapes and sizes of photonic structures, at CEA-Leti, we have incrementally developed a DRC that applies component specific rule subsets, one of which applies directly to our fibre grating couplers.

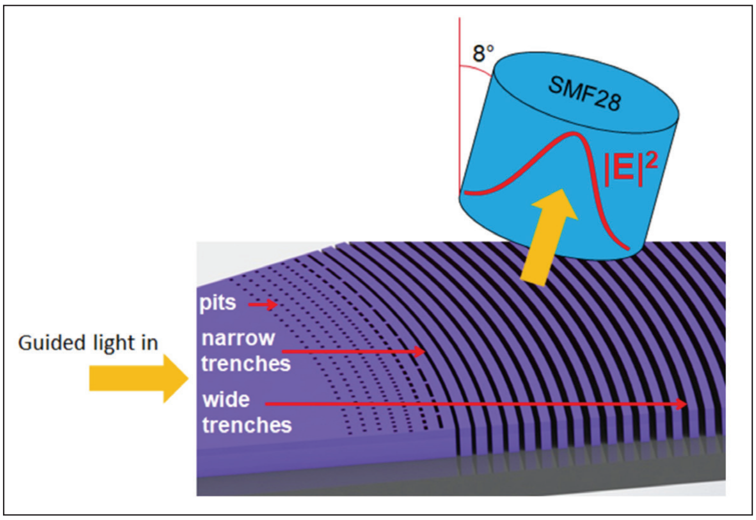

Figure 1. General architecture of the CEA-Leti O-band fibre grating coupler. Incoming guided light is scattered by a non-uniform, curved diffraction grating into a single mode fibre placed above at 8° to the vertical.

Once past the DRC stage, the target design layout must then undergo a post treatment process designed to compensate for unavoidable geometric distortions induced by the fabrication process. This treatment is known as Optical Proximity Correction (OPC) and is routinely applied in the CMOS industry. However, as for DRC, off-the-shelf OPC software is based on algorithms optimised for Manhattan-style electronic structures and is not well suited to the curvilinear structures found in photonics[5].

Figure 2a shows an image of a grating coupler, fabricated in 2013, with a similar design to that in Figure 1, using nominal process conditions on a platform without OPC. The pits are not present and the finest trenches are poorly defined. Figure 2b shows a typical layout before and after OPC (grey boxes and black lines, respectively), as well as the simulated result of the etched grating structure (red boxes). Figure 3 shows a later fabrication run with

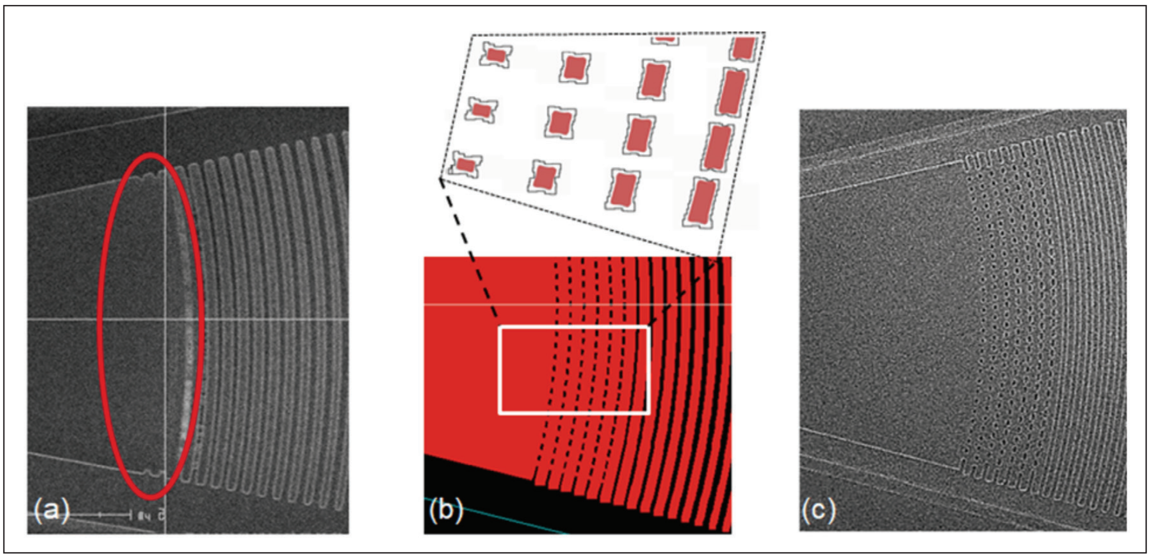

Figure 2a. Image of device fabricated in 2013 without OPC treatment, with missing features. 2b. OPC treatment of target design, the black lines show the post-OPC layout. 2c. Image of device fabricated in 2018 using OPC.

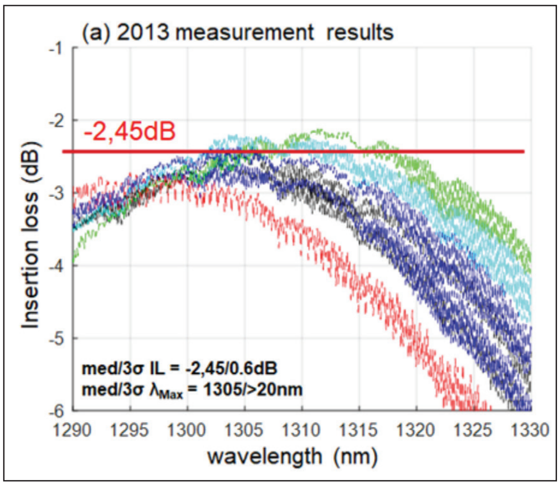

Figure 3a. CEA-Leti fibre coupler Insertion loss measured in 2013.

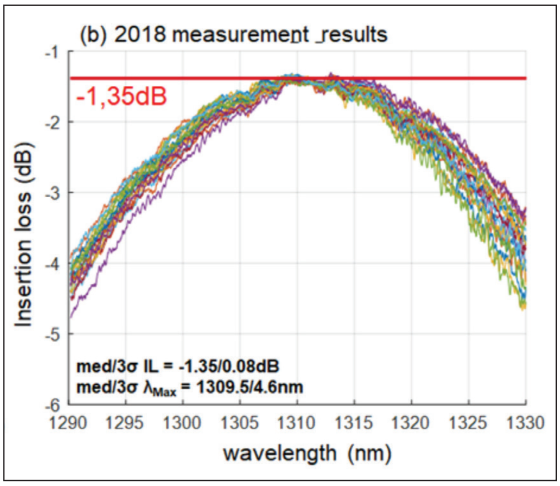

Figure 3b. CEA-Leti fibre coupler insertion loss measured in 2018 following iterative improvements in design, process and testing

an optimized OPC treatment in which the diffraction grating is correctly defined.

Another crucial contribution the development of the fibre grating coupler and of the photonic design-kit in general is a means of precise, reproducible and automated device characterization. Unlike obtaining insertion loss values of other photonic devices in which fibre coupling losses can be subtracted using a suitable reference structure, measuring the insertion loss of the coupling structure itself is subject to greater uncertainty. Like the layout tools described above, dedicated hardware for testing PICs is slowly coming to the market (e.g. www.ficontec.com,www.cascademicrotech.com), but as mentioned previously, achieving automated characterisation is another area where CMOS electronics hardware has had to be significantly modified for photonics applications.

At CEA-Leti, our wafer-scale characterization benches are based on CASCADE prober stations with piezo-mechanic fibre holders, which provide rapid (~100ms) submicron active lateral alignment, together with active fibre height control and polarisation control. We estimate the measurement precision and reproducibility of our system to be around 0.1-0.2dB.

Figure 3a shows a measurement made in 2013 of the IL spectra of our nominal CEA-Leti fibre grating coupler over the wafer surface. The median minimum insertion loss is -2.45dB. A 2018 measurement, shown in figure 3b, shows a marked improvement in IL, with a medium value of 1.35dB. The coupler design was very similar in both cases, the difference is due to enhanced lithographic control and a functioning OPC. Furthermore, the reduced dispersion over the wafer of the minimum insertion loss value ($3\sigma=0.08$dB, c.f. $3\sigma=0.6$dB) in the 2018 data can be attributed to a combination of improved process control (notably the stability of the partial etch step) and stability of the measurement system.

Conclusion and prospects

Several key aspects of the development of the CEA-Leti fibre grating coupler have been presented. Using this as a case study, we seek to illustrate just a few of the many ways in which silicon photonics, while using the same set of materials and process techniques as in CMOS electronics, has required, and continues to require, significant development in order to fully exploit the economies of scale available to CMOS electronics.

At CEA-Leti, we are currently introducing immersion lithography to have access to finer lithographic control. This will allow the use of more aggressive grating designs and potentially lower fibre coupling insertion loss.

For more information on CEA-Leti visit:
www.leti-cea.com/cea-tech/leti/english/Pages/Applied-Research/Strategic-Axes/optics-photonics.aspx

Further reading

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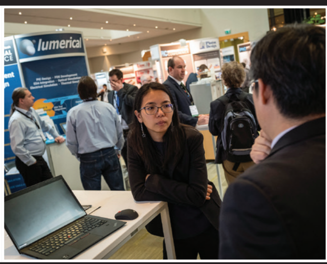


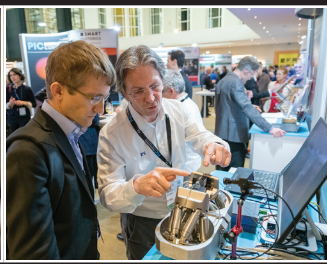


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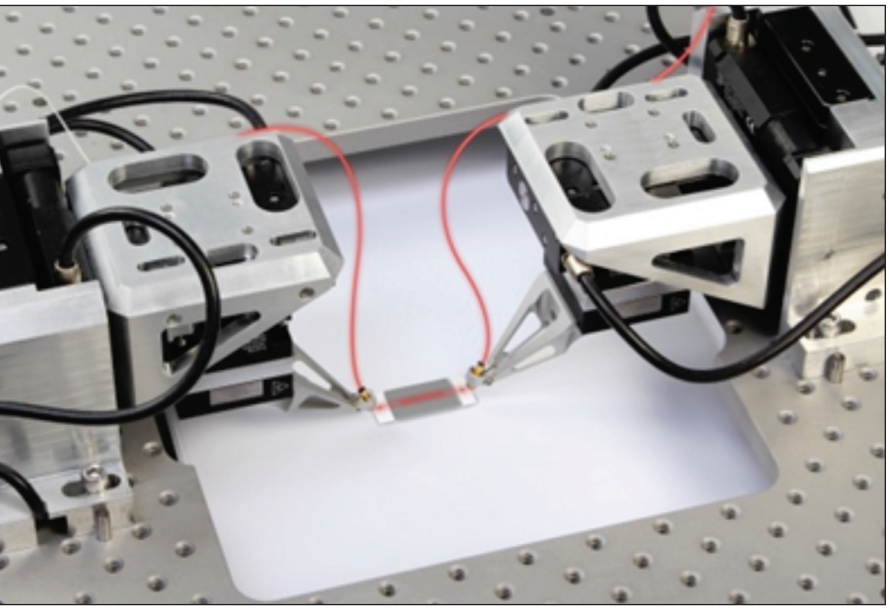
Practical examples of parallel **photonics alignment automation**

Physik Instrumente address challenging PIC / SiP requirements by automating processes that today are often done manually.

By Scott Jordan Sr. Director, NanoAutomation Technologies, Head of Photonics, PI (Physik Instrumente) L.P.

AUTOMATED TEST, assembly and packaging (TAP) is seen by most across the photonics ecosystem as a 'gate' through which designers, developers and manufacturers all must pass along the road to achieving profitability. A significant part of the growth potential projected for silicon photonics (SiP) or PICs hinges on miniaturized, high-performance optical devices entering markets that will grow to high volume relative to their current levels. But there's a catch: To achieve success here means that quality excursions and warranty losses so common with first generation 100 Gbps transceivers must be brought within industry norms. PIC and SiP devices must also transition to standardization and other QC-methodologies designed to help companies achieve improved device performance and repeatability at scale.

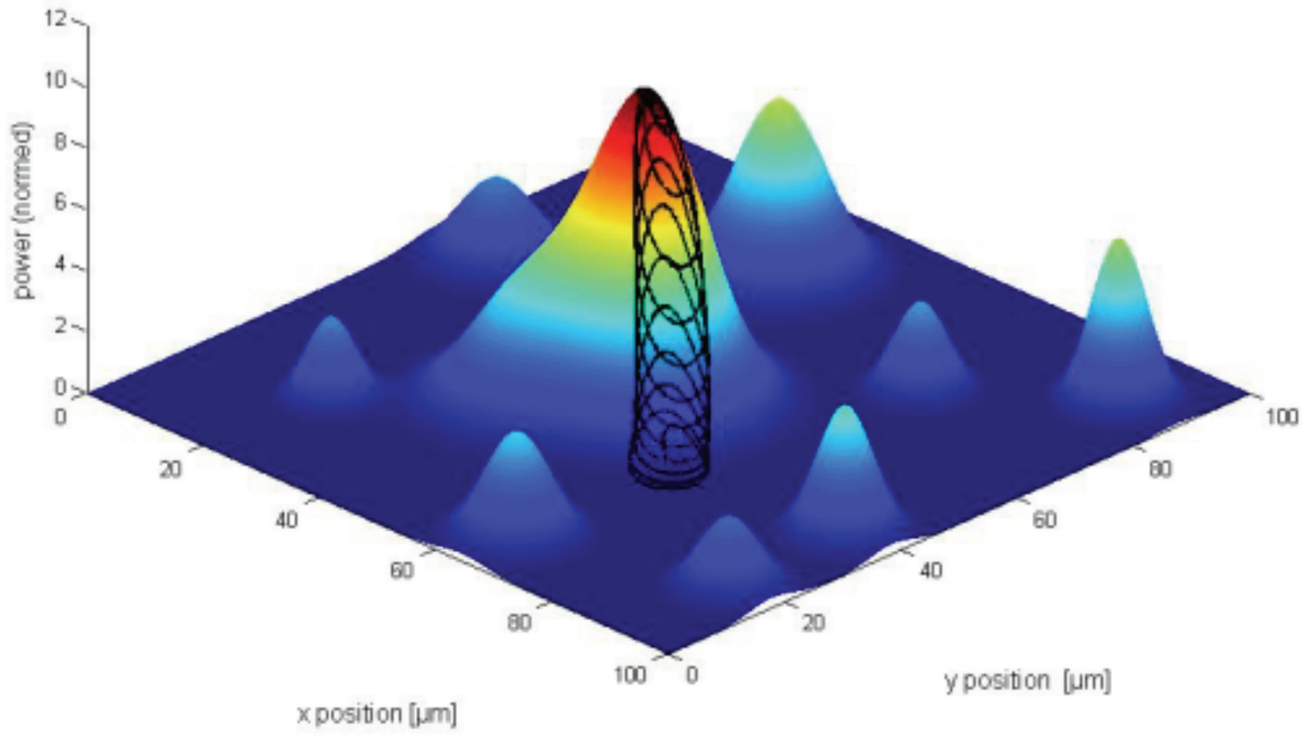


Achieving high-volume manufacturing levels is essential to the long-term growth and vitality of photonic markets to minimize risk and maximize revenue potential essential to achieving PIC placements beyond datacom inside LiDAR / automotive, other photonic sensor systems, digital cameras and smart phones.

Physik Instrumente continues to expand its TAP portfolio to address challenging PIC / SiP requirements by automating processes that today are often done manually. Manual assembly and test frequently introduce incons istences that can lead to quality excursions while also being painstakingly slow compared to automated solutions. *PIC Magazine* editors invited experts from PI to discuss market requirements and their solutions that can improve throughput and accuracy up and down the production line whether in research settings or higher volume production environments.

Fast, Multi-Channel Photonics Alignment (FMPA) technology, developed by Physik Instrumente, is a set of firmware-level commands built into extremely high-performance digital nanopositioning and hexapod controllers. These commands allow fast

Figure 1: Aligning the inputs and outputs of waveguide devices at an industrial pace requires parallel optimization and nanoscale accuracy. (Image PI)



Serial versus parallel alignments

For example, in the short waveguides increasingly utilized in Silicon Photonics (SiP) devices, the input and output couplings can steer each other. As one side is optimized, the other shifts slightly and needs re-optimization. Formerly, this necessitated a time-consuming, serial sequence of back-and-forth adjustments of the input, then the output, repeating until a global consensus alignment was eventually achieved. Similarly, when optimizing an angle, the transverse alignment would be impacted and would conventionally need to be re-optimized, again in a time-consuming serial loop.

coupling optimization between photonic and other optical devices and assemblies, including optimization across multiple degrees-of-freedom, inputs and outputs, elements and channels. Importantly, these optimizations can often be performed in parallel, even if the individual optimizations interact. Examples where significant process savings can be achieved span the spectrum from multichannel Silicon Photonics devices to LIDAR sensors to smartphone camera assemblies.

But with FMPA, these interacting alignments can often be optimized simultaneously, in parallel. This allows a global consensus alignment to be achieved in one go. Tracking and continuous optimization of all the alignments is also possible in many circumstances, allowing compensation of drift, curing stresses, and so on.

The results are much higher production throughput and often dramatically lower costs. As devices become more complex and precise, and as their production and test requirements grow more demanding, this parallelism is increasingly critical to process economics.

Look for the loops

Fully exploiting this capability for maximum overall cost savings can require some different thinking than what one might be used to with classical alignment hardware. In general, one looks for loops of sequential alignments, for which simultaneous optimizations can usually be substituted.

This article reviews a few sample applications and discusses implementation issues to illustrate how this remarkable new capability can be utilized to maximize productivity in test and packaging.

Background of FMPA operation

The device alignment should be broken down into discrete alignment processes. For example, probing a waveguide with one input and one output using lensed fibers typically involves four alignment processes:

1. Transverse optimization routine, input;
2. Transverse optimization routine, output;
3. Z optimization routine, input (beam waist seek);
4. Z optimization routine, output (beam waist seek).

Figure 2: F-712.MA2 high precision fiber alignment system. (Image PI)

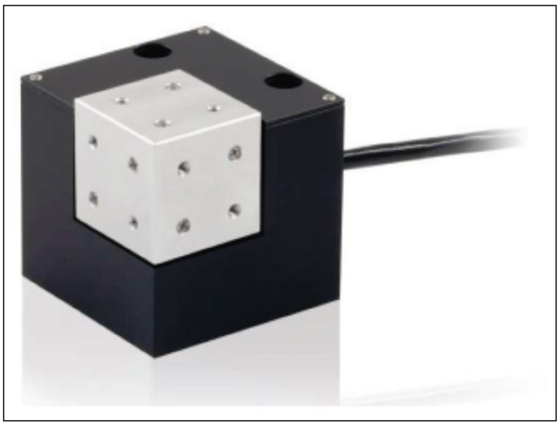


Figure 4: NanoCube®, piezo-based, high dynamic, 3-axis scanner with 100 µm travel range. Besides its nanoscale resolution and blazing speeds, this flexure-based subsystem can perform continuous tracking without wear. (Image PI)

If the device has one or more additional inputs or outputs, add as necessary:
5. Theta-Z optimization routine, input;
6. Theta-Z optimization routine, output.

If the device requires optimization in theta-X and theta-Y, add:
7. Gimbaling optimization routine, input
8. Gimbaling optimization routine, output.

And so on. Dividing the overall alignment task into these sub-processes is key to identifying which processes can be performed simultaneously.

With FMPA, you take the list of alignment routines and define these directly into the controller. This only needs to be done once (and can be changed or updated at any time). Once a routine is defined, it can be executed repeatedly. You can execute more than one routine at a time – this is the parallelism.

Defining a process means instructing the controller which axes are involved in the process, which analog input presents the quantity to be optimized (optical power, MTF…), and various process options. Give each process a name… the numbers in the list just made are perfect for that.

Routines are executed by calling the Fast Routine Start command, FRS. Referring to the list just constructed, FRS 1 would commence the transverse optimization on the input. FRS 2 would commence the transverse optimization on the output. And FRS 1 2 would do both at once.

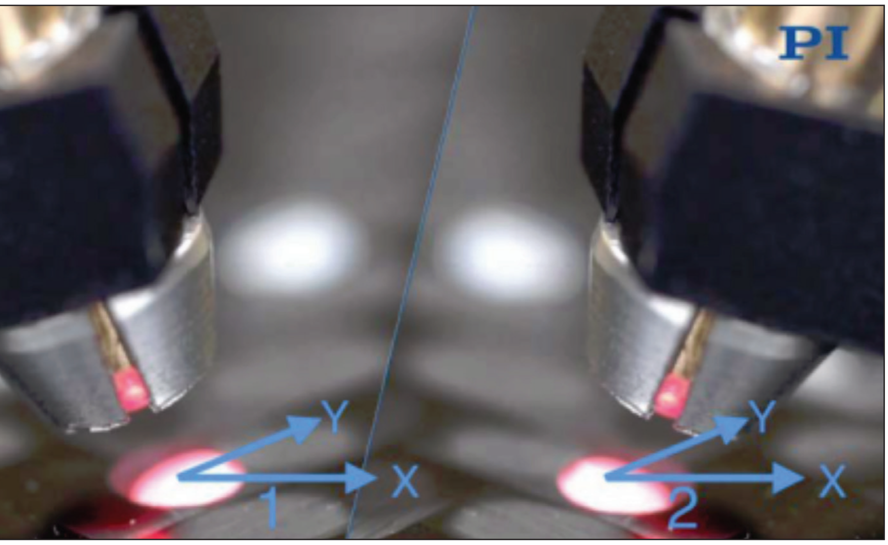


Figure 3: Dividing a task like waveguide I/O coupling into sub-tasks like "1" and "2" (shown) will illuminate opportunities for parallel execution. Here, the two processes can proceed in parallel even though they interact, especially in the case of short waveguides where inputs and outputs steer each other. Similarly, processes related geometrically (such as a transverse and Z optimization in situations such as shown, with an angled beam) can be performed in parallel. (Image PI)

Types of alignment routines

For each side of the device, independent alignment engine hardware is, of course, necessary. Any number of alignment engines can be used; most common configurations utilize one or two, but three or more will be increasingly common as SiP technology matures.

Most often, each alignment engine is constructed of a multi-axis long-travel assembly and a shorter-travel, high-speed, high-resolution piezoelectric multi-axis nanopositioning stage. The modularity of the approach is a key benefit. Some applications do not require the long travel mechanism; some applications do not require the speed, resolution or continuous tracking capability of the nanopositioning stage. In any case, all FMPA algorithms and processes are virtually identical regardless of the type of motion system involved; only the capabilities will differ.

Long travel options

For situations requiring no angular optimizations or array alignments, a stack of linear stages is sufficient. Otherwise a hexapod is required – not only in situations where full six-degree-of-freedom positioning and optimization is necessary, but also in simpler situations, as the hexapod allows the rotational centerpoint of even a single angular optimization to be

Figure 5: Single-sided fiber alignment system. (Image PI)

placed on the optical axis, at the beam waist, etc. This is vital for reducing parasitic geometric errors, another key to improved overall productivity. Sometimes very long travel is necessary in one or two axes for loading operations, and in these cases the hexapod can be mounted on a long-travel motorized stage. (The hexapod controller accommodates two additional DC-servomotor axes. Alternatively, force-sensor elements can be integrated.)

The alignment processes

There are two types of processes: areal scans intended to localize a peak within a defined region, and gradient searches intended to efficiently optimize coupling (and optionally track it to mitigate drift processes, disturbances, etc.).

Gradient searches

Gradient searches perform a small circular dither motion of one device versus the other, which modulates the coupling. The amount of modulation of the figure-of-merit being optimized (for example, optical power or MTF) is a measure of the local gradient of the coupling. The modulation falls to zero at optimum (Figure 6).

$$|\varepsilon(\theta)|=\nabla I=(I_{min}-I_{max})/I_{min}$$

Equation 1: The observed gradient serves as a measure of alignment error. (Image PI)

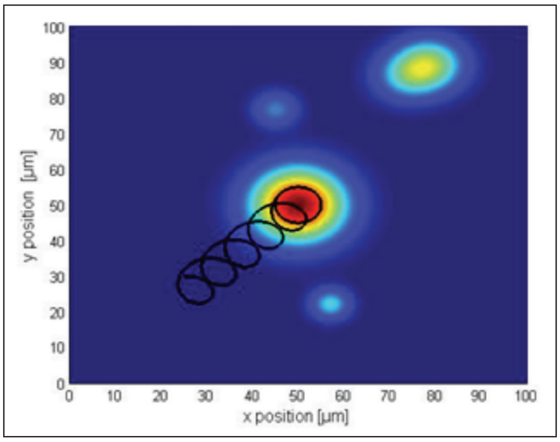


Figure 7: Optical power distribution. (Image PI)

From the observed modulation you can mathematically deduce the local gradient via a very simple calculation, such as Equation 1. Note that the gradient ∇I falls to zero at optimum.

Any axes in an FMPA system can perform any of these types of alignments (subject to the physical capabilities of the axes, of course). So, areal scans can be performed with motorized-stage axes,

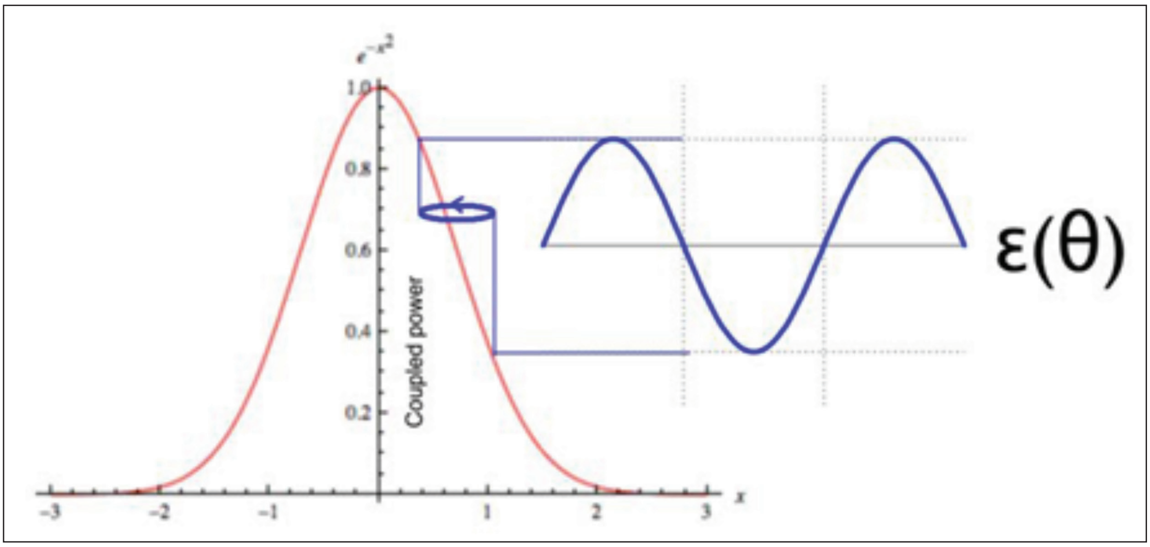


Figure 6: Graphical depiction of gradient determination via a circular dither, which modulates the coupled power (or other quantity) observed. The phase of the modulation with respect to the dither indicates the direction towards maximum while its amplitude falls to 0 at optimum. (Image PI)

which can be very handy for finding first light. Gradient searches are most familiar from transverse optimization, but they can also be performed (for example) in a single linear axis, which is ideal for localizing the beam waist in a lensed coupling, or in a gimbaling fashion to optimize an angular orientation. There are many possibilities. These are highly general-purpose algorithms suitable for all kinds of optimizations, including bulk optic, cavity and pinhole alignments.

In general, a unique feature of FMPA is that different gradient searches can be performed in parallel. Transverse optimizations tend to be the most sensitive and also the most affected by other alignments. So, transverse routines tend to be relegated to high-speed, high-resolution piezoelectric stages such as PI's P-616 NanoCube. The high speed and continuous tracking capability of the NanoCube allows transverse optimization to be maintained during Z and angular optimizations that would ordinarily require the time-consuming, looping sequential approach.

Areal scans

Scanning an area to determine the approximate location of the highest coupling peak is useful for a variety of tasks:

- First-light seeking;
- Profiling for dimensional characterization of a coupling. This can be an important process-control step;
- Localizing the main mode of a coupling for subsequent optimization by a gradient search. This hybrid approach helps prevent locking-onto a local maximum and is very powerful.

In addition to reducing the areal scan to a single command, FMPA controllers have automatic curve-fitting capabilities built in, plus a data recorder that can capture the profile on-the-fly for later retrieval, analysis or databasing. FMPA areal scans are very fast, 300 msec or so for typical NanoCube applications and loads. The curve-fitting capability can fit a Gaussian to a fairly sparse scan (meaning an especially fast scan), allowing good localization of the optimum coupling point without taking a lot of time to do a really fine scan.

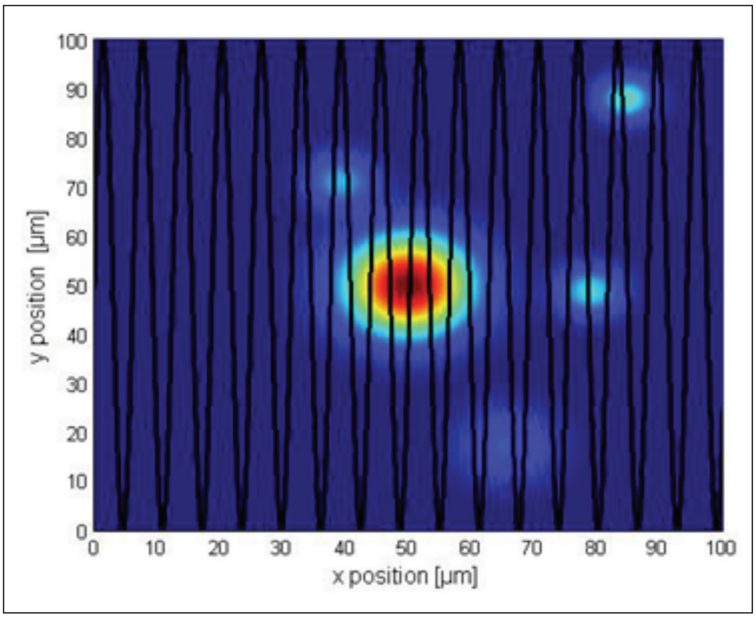


Figure 8: Optical power distribution. (Image PI)

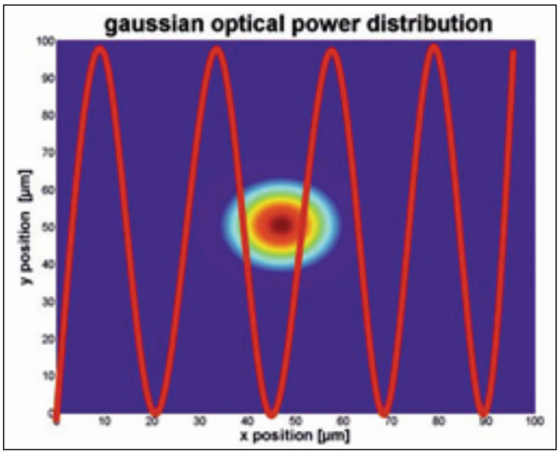


Figure 9: Sinusoidal area scan. (Image PI)

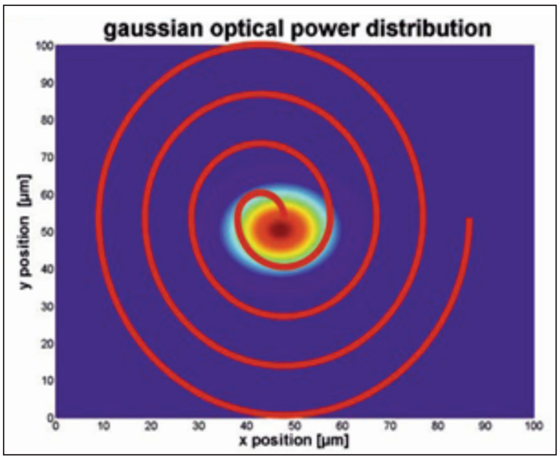


Figure 10: Spiral area scan. (Image, PI)

Another capability is finding the centroid of a flat-top (top-hat) coupling, such as seen when probing a deposited photodetector with a single-mode fiber. This allows the scan to terminate with the fiber at the geometric center of a flat or tilted top-hat coupling.

Uniquely, FMPA's areal scan options include single-frequency sinusoid and spiral scans. These are much faster than traditional raster or serpentine scans since they are truly continuous and avoid the settling requirements of the stop-and-start motions used in the traditional scans, and the frequency can be selected to avoid exciting structural resonances.

A constant-velocity spiral scan may also be selected, allowing data to be acquired with constant density across the spiral.

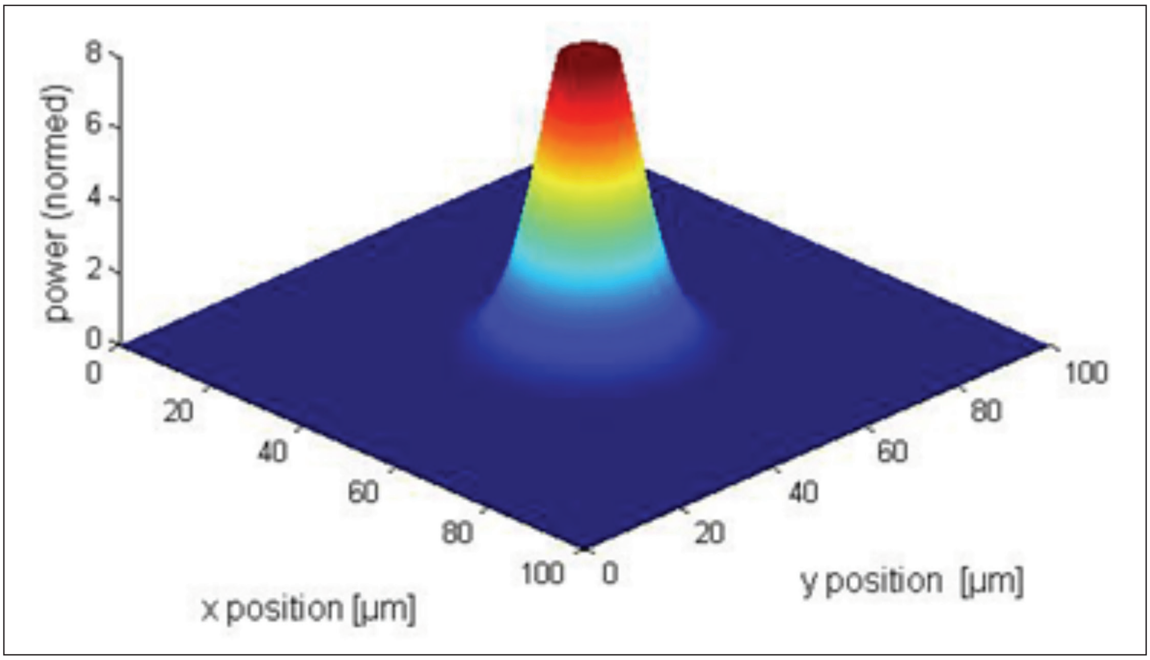


Figure 11: Uniquely, PI FMPA controllers can perform a fast areal scan and automatically calculate and align robustly to the centroid position of upright and tilted top-hat couplings. (Image PI)

Example 1:
Wafer Probing of Angle-Insensitive Devices

Even in the simplest case of a short waveguide device with just one input and one output, the steering interaction mentioned above can present a frustrating process bottleneck. Add the additional alignments necessary for angle-sensitive couplings and array devices, and the situation would grow complex and time-consuming very quickly. Parallelism mitigates all this and makes short work of the task.

For this example, let us first consider a planar waveguide device with a single input and single output, both accessible for probing via diffractive couplers. Many thousands of such devices are commonly fabricated on large wafers, so throughput is very important. The diffractive couplers typically project the waveguide's input and output out of the wafer at a typically 10-25° angle from the vertical.

Often, lensed probe fibers are used, so there is a fairly distinct optimum separation along the optical axis. Wafer probers of good quality provide wafer placement accuracies much less than the 100 µm × 100 µm × 100 µm field of view of the NanoCube, so first light seeks are generally not needed on a per-device basis in probing applications.

Note that the optical Z axis is at an angle to the mechanical Z axis for normal mounting of the stage stacks:

$$Z \text{ optical} \nparallel Z \text{ mechanical}$$

Usually it is not desirable to tilt the motion assembly to accommodate the angled optical beam since the mechanical XY plane should remain parallel to the wafer to avoid collisions. Consequently, optimization motions in mechanical Z must be accompanied by compensating motions in X and Y to keep everything aligned.

This is an ideal case for parallelism. From the generic list of alignment routines, compiled above, the first four apply:

1. transverse optimization routine, input;
2. transverse optimization routine, output;
3. Z optimization routine, input (beam waist seek);
4. Z optimization routine, output (beam waist seek).

Using traditional, non-parallel alignment technology, the conventional approach would be:

1. To accommodate Z optical $\nparallel$ Z mechanical, loop:

a. To accommodate steering effects, loop:
   i. Align one side to maximize throughput;
   ii. Align the other side to maximize throughput.

Figure 12: E-712 digital piezo controller. (Image, PI)

b. Move in Z and evaluate if the move direction improved coupling.

2. Repeat the above loops until optimized. Overall time required is often many tens of seconds.

Using FMPA, the process is much simpler and can be two or more orders of magnitude faster. Fundamentally, one defines gradient searches 1 – 4 from the list (again, this only needs to be done once, though any process can be modified or re-defined freely), and then for each device:

- Issue the Fast Routine Start command: FRS 1 2 3 4

Execution is typically complete in a few hundred msec.

A single E-712 controller supports up to four P-616 NanoCubes, which can even be deployed on different workstations – they do not all need to be processing the same device.

Tracking and the completion criterion

A signature advantage of the gradient search is that it cannot only optimize but also track its optimum. If you have several gradient searches operating on a device, all can track simultaneously. Alternatively, for your application you may wish to align and then stop and hold position at the optimum.

This criterion – whether to align-and-stop or keep tracking – is an example of a parameter you can adjust in the process definition to fine-tune the process' behavior to meet your application goals; there are many such options.

Since the process depends on the instantaneous gradient of the coupling, it is natural to define its stop point in terms of the gradient. We call this the Minimum Level, or ML. Setting the process' ML parameter to 0 means it should never be satisfied and should track until commanded to stop.

This is very useful for accommodating drift processes, such as in elevated-temperature testing. Setting ML to a small, but non-zero value, causes the gradient search to terminate at the observed optimum position. Note that ML = 0 tracking should only be performed with flexure-guided mechanisms due to the potential for mechanical wear in mechanical mechanisms.

Example 2: Wafer Probing of Angle-Sensitive or Array Devices

Building on Example 1, you can accommodate angle-sensitive devices and array devices by using a hexapod rather than an XYZ stack of stages for the long travel motion. For many applications a hexapod will provide sufficient resolution and speed, otherwise (or when continuous tracking is needed) a NanoCube can be attached. Again, the modularity of the FMPA architecture yields considerable flexibility.

Alignment hexapods have many advantages over a stack of conventional linear stages and angular positioners such as goniometers. First, hexapods are full six-degree-of-freedom devices, and their rotational centerpoint is freely settable anywhere in space. This means you can rotate about a fiber tip, a beam waist, a waveguide axis or any other optically desirable point in space.

PI hexapods present a sensible Cartesian coordinate system to the user (X, Y, Z, θX, θY, θZ) and allow you to easily cast and rotate that coordinate system as desired. Among other things, this means you can mount a hexapod on an angle bracket to minimize overall footprint, while still having an XY scan plane parallel to a wafer or other important datum surface.

Again the FMPA areal and gradient search capabilities (for linear and angular axes), data recorder and profile fitting functionality is built into the controllers, yet costs are typically less than a stage stack of equivalent resolution and motion performance.

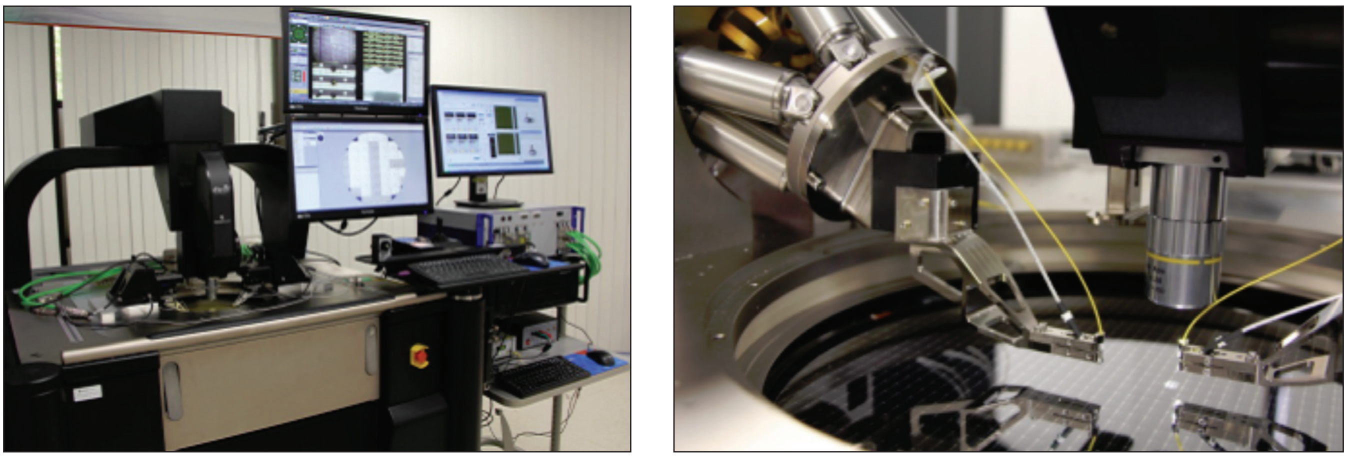


Figure 13: Cascade Microtech's pioneering CM300 photonics-enabled engineering wafer prober integrates PI's Fast Multichannel Photonics Alignment systems for high throughput, wafer-safe, nano-precision optical probing of on-wafer Silicon Photonics devices. Left: XYZ prober configuration. Right: 6-DOF hexapod perober configuration. (Image, Cascade Microtech, division of Formfactor, Inc.)

Consider the case of an on-wafer device with an array input, output or both. On the sides with the arrays or other angle-sensitive elements, the hexapod-based alignment engine is mounted. Using traditional, non-parallel alignment technology, the conventional approach to optimizing this would utilize an even more complex looping sequence:

For the first channel...
a. To accommodate Zoptical ≠ Zmechanical, loop:
To accommodate steering effects, loop:
- Align one side to maximize throughput.
- Align the other side to maximize throughput.

b. Move in Z and evaluate if the move direction improved coupling.

c. Repeat the above loops until optimized.

- Increment in θZ. It is unavoidable that the transverse alignment will be degraded by this.
- Repeat (A). Evaluate if the increment improved coupling in the Nth channel.
- Repeat (A) - (C) until the both the first and Nth channels are optimized. For most applications this will mean the entire array is optimized.

Overall time required is typically multiple minutes.

Using FMPA, the process is again much simpler and vastly faster. As in Example 1, one defines gradient searches 1 – 4 from the list, and then defines either a single-axis sinusoidal ("areal") scan or a gradient search in θZ. Let's call this process 5. (The gradient search requires some initial coupling, but the areal scan does not, so the choice of one or the other depends on the application, fixturing, device consistency, etc. Also, setting soft limits to prevent a gradient search from walking away if optical power is cut is both prudent and easy).

There are additional options and parameters that should be considered in an actual application. This overview should provide confidence that the productivity of parallelism is accessible in many applications

Then, for each device…
- Set the NanoCube to track continuously (ML=0 for processes (1) - (4)) for the first channel. Issue the Fast Routine Start command: FRS 1 2 3 4.
- With the NanoCube tracking the transverse and Z couplings on both sides of the waveguide, issue the Fast Routine Start command for the θZ process 5.

Execution is typically complete in less than a second. Addressing gimbaling (θX/θY) alignment is similarly simple and fast with FMPA.

Summary

This is intended to be an illustrative, but not exhaustive description. Similar sequences can be quickly devised for packaging, chip-test and other applications. There are other ways of performing each of the examples we have presented, and application considerations may recommend different approaches or modifications. There are additional options and parameters that should be considered in an actual application. This overview should provide confidence that the productivity of parallelism is accessible in many applications.

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DATES, THEMES AND FIRST SPEAKERS ANNOUNCED!

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Attracting more than 700 delegates, consisting of co-located Compound Semiconductor International, and Sensor Solutions International, plus a single exhibition area, delegates can dip in and out of every session to put together their own tailor-made programme by selecting from over 125+ invited talks, delivered by leaders of the most innovative global companies of today.

With a strong synergy between the three conferences, attendees and exhibitors are fully exposed to the relevant supply chains as well as customer and supplier bases.

The PIC International Conference continues to grow in scale nd stature year on year and is now firmly established as the must-attend conference for the PIC industry. With an attendance in 2019 of 700 senior level delegates including representatives from Facebook, Intel, IBM, and the European Commission among many others, the event was our largest yet.

Preparations for PIC International 2020 have got off to a fantastic start, with a record number of industry leading speakers and sponsors already confirmed for the event with 8 months to spare.

5 New Themes for 2020:

PICs Today - Datacom, Sensing & LiDAR

Datacom remains today's largest PIC opportunity. We will explore progress in PICs for data switching / transmission along with the potential for PICs in emerging sensing applications including LiDAR, digital imaging, fibre optic sensors and bio-photonics.

PIC Manufacturing - TAP, Co-Packaging & Fab

As early generations of PICs are moving into commercial applications the need for automated test, assembly and packaging (TAP) is paramount to ensure long-term reliability. Opportunities for co-packaging hold promise while foundry consolidation and applications beyond datacom have implications for substrate suppliers, EDA/EPDA and many others across the supply chain.

PIC Technology - Solutions, Analysis & Research

The rapidly evolving nature of photonic integration, silicon photonics (SiP), optical computing and automotive SoCs tied to PICs offers new manufacturing opportunities. We will explore programmable PICs, the coherent vs. incoherent debate, quantum encryption and the latest integration/hybridization approaches for light sources and other PIC devices.

PIC ROI - Quality Metrics & Scalability

Scalability is a key manufacturing interest as pilot lines set the stage for volume manufacturing. What metrics can best be applied to design and manufacturing as the industry pivots to higher production levels? Is a total quality management (TQM) approach vital to long-term vitality? We'll explore TAP within a quality matrix and how today's systems can be readied for long-term scalability and margin growth.

PICs Vision - Evolution and Revolution

As PICs move from 100G to 400G, the future will require 800/1600G devices - can we set the stage today for a smooth transition? We will explore leading pathways to a PIC-enabled future and what needs to be initiated in the short-term to satisfy long-term requirements. What role might quantum technologies play to increase performance, reduce power consumption and improve quality?

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The fascinating ways digital olfaction is being used across industries

"If you are ambitious to find a new science, measure a smell," said Alexander Graham Bell, famously. **Tristan Rousselle, Founder & CEO, Aryballe Technologies** discusses the broad and far-reaching applications of this powerful PIC-enabled MEMS technology.

ALEXANDER GRAHAM BELL was adamant human smell could not be reproduced, but that hasn't stopped decades of researchers from attempting to evaluate and quantify odor using electronic noses. In fact, the first concept of an electronic nose appeared in the 1950s, introduced by J.D. Hartman, a scientist researching flavors in vegetables. Later, in 1982, thanks to the invention of the first gas multi-sensor array, that concept started to take shape and become more reality than idea.

The technology behind electronic noses, digital olfaction, is generally defined as the digital capture and production of aromas, and its applications are broad and far-reaching. Similar to our sense of smell, digital olfaction mimics the process by which our brains identify and differentiate between odors. But to understand how it works, we must first define odor.

What is an odor?

Objects release odor molecules in response to energy variation. When energy increases (through temperature, agitation, pressure, etc.), evaporation of an odor occurs, and it then becomes possible for humans to absorb this odor through their nasal cavities. This stimulates the neural system of the olfactory bulb, and using other information, such as memory, the olfactory cortex produces the final result: the smell of the object.

Digital olfaction, therefore, binds odor molecules to bio-sensors, which act as the olfactory bulb, and produce a unique odor signature. New innovations in MEMS technology are enabling the deployment of hundreds of sensors simultaneously to better discriminate between different odors. This represents a huge leap forward for digital olfaction—taking the potential for this technology out of the lab and into everyday lives.

The benefits of MEMS technology

MEMS technology, traditionally used for telecommunications bandwidth applications, provides an important layer of functionalization for generating a digital pattern. MEMS are often more robust than traditional gas sensing techniques and can support dozens of bio-sensors rather than one. Our MEMS platform is based on interferometry and uses photonic integrated circuits (PICs) in its construction.

The sensors capture odor molecule responses with peptides to create the unique odor signatures. The platform also lowers the cost of manufacturing as many of the tools for MEMS technology were developed more than two decades ago for semiconductors used in microphones, telecoms and cameras. Those tools can be reused today for the production of digital olfaction sensors, eliminating the need for companies to create or manufacture their own class of tools.

Despite the potential for MEMS technology in odor sensors, many digital olfaction technologies on the market today continue to only use gas sensing techniques that are limited in the capture of odor data. To effectively replicate the human sense of smell, the sensor needs to detect the odor signal through a combination of peptides in order to capture the inherent multi-dimension nature of smell.

The nose reproduced

Once the odor signatures are detected, which occurs as result of electrostatic interaction that triggers a reaction between the odor molecule and biosensor, software then interprets those signatures based on a database of previously collected and analyzed odors. Think of this almost as our memory bank, which our brains rely on to correlate individual smells to life and learning experiences to classify the odor accordingly.

While the technology may not yet have the same sophistication of the human olfactory system, new advances in digital olfaction are making it easier for companies to innovate and enter the space. Notably, we've seen several devices come to market that focus on air control and breath analysis. Alphaszensor, the developer of the CNTnose, detects gaseous biomarkers through human breath and is currently addressing applications in identifying infectious diseases. Peres, the developer of Foodsniffer, is focused on food poisoning and preventing foodborne illnesses.

But beyond health and wellness, digital olfaction plays a key role in quality control, specifically in three core industries: food & beverage, home appliances, and automotive.

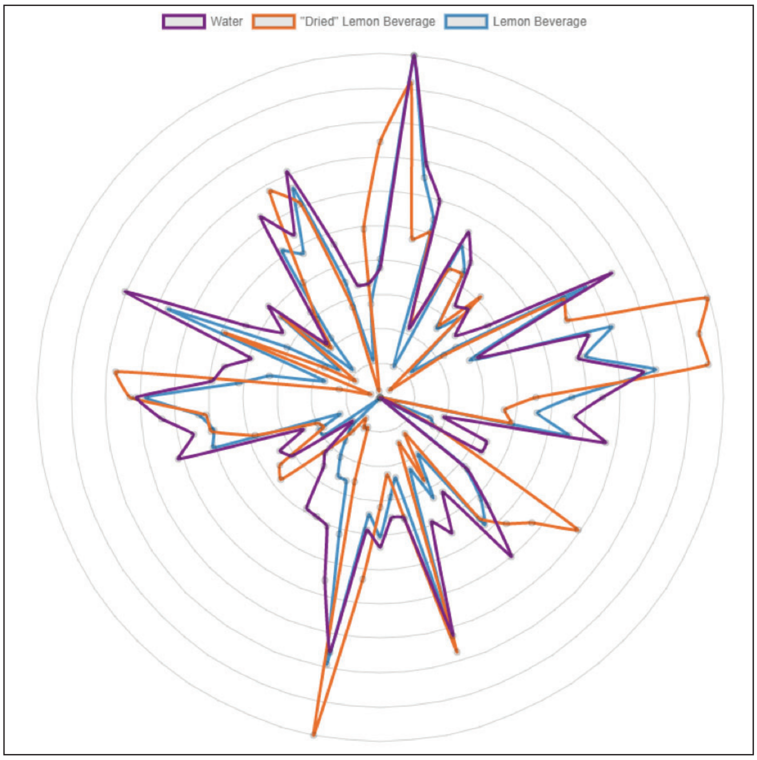

Figure 1: The above graph demonstrates how the scent of lemon would appear digitally – both in its raw diluted form in water and also with advanced humidity analysis ("Dried" Lemon Beverage). By using the software analytics component of digital olfaction, the solution takes into account the odor impact of water and isolates the lemon odor from it. Manufacturers would want to consistently see the same lemon olfaction pattern over and over again to ensure the same odor and thus flavor of the lemon beverage.

The food & beverage industry

One of the top use cases for digital olfaction involves quality assurance or quality control to either maintain controlled conditions or ensure consistency in manufacturing. For example, as consumer demand for sparkling water beverages grows, manufacturers must ensure the flavor, a combination of taste and smell, can be replicated time and again to ensure customer satisfaction.

At the same time, flavor contamination from food packaging is a recurring issue. Digital olfaction can help to prevent this "flavor scalping" by monitoring when food starts to absorb aromas from packaging, or even help manufacturers add the scent of the food item to packaging materials.

Inside our home appliances

Homes today are stocked with numerous smart appliances, from controlling temperature to entertainment and security. So, it shouldn't come as a surprise that appliance manufacturers are also interested in devices that can smell. The more common (household) use cases take place in the kitchen, with refrigerators outfitted with odor sensing technologies that can alert consumers when food is about to go to waste. In fact, we've examined this exact scenario using a digital olfaction sensor device, which we used to determine whether a piece of fish had begun to spoil (Figure 2). As suggested by the graph below, digital olfaction helps to categorize food using pattern recognition, comparing the food item's current odor signature to previously collected odor data to identify whether it is fresh or rotten.

The same process could apply to other appliances, such as an oven that would automatically stop when food is cooked or has reached its preferred level of doneness. We've seen digital olfaction devices distinguish between cookie dough and a baked cookie, all by relying on the odor data collected.

The automotive world

Odor sensing technology in vehicles offers numerous use cases, many of which are already being explored. The Digital Olfaction Automotive Consortium (DOAC), launched in March 2019, was created to address industry trends attributed to new mobility services and the evolution of self-driving cars. Together, Aryballe Technologies and the consortium's founding members, including DENSO, will establish the standards for odor measurement in the automotive industry and inform olfaction product development

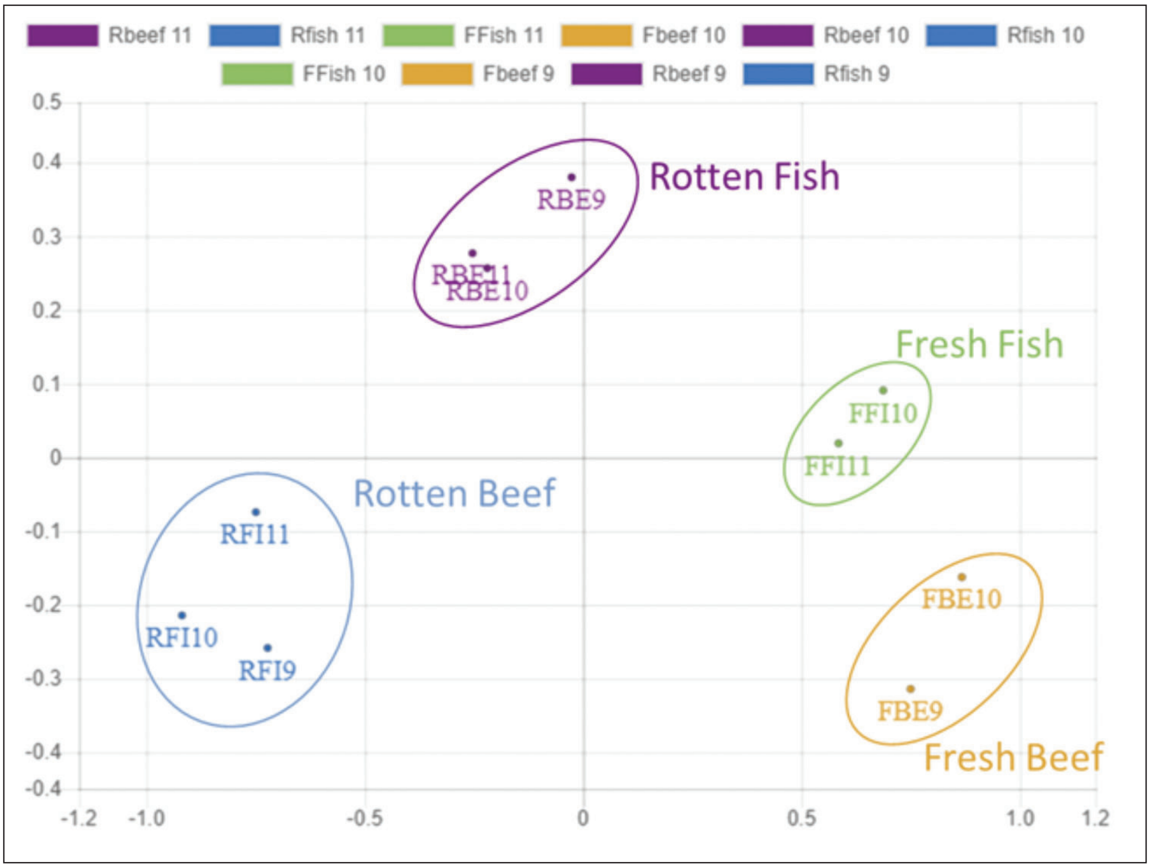

Figure 2: A graphical representation of data collected through digital olfaction. Suitability for consumption is illustrated as a continuum along which various foods are described as 'fresh' or 'rotten' based upon predetermined olfactory markers that represent the foods' age / freshness and other characteristics.

and services. That involves everything from detecting nuisance smells and component malfunctions, which could include everything from stale food to a fuel leak, to helping refresh the smell of vehicles involved in peer-to-peer car-sharing.

Continued advances in digital olfaction will produce many more applicable use cases beyond what we've highlighted here. Digital olfaction not only provides consistency in the definition and use of smell, but enables companies to use odor data collected to inform key business decisions, from rejecting or approving a raw material supply, to reducing analysis time in the R&D formulation of a new beverage by outlining whether the new formula tastes similar to the original. Needless to say, the digital olfaction industry will continue to grow in the near future, and soon will be present in everyday life.

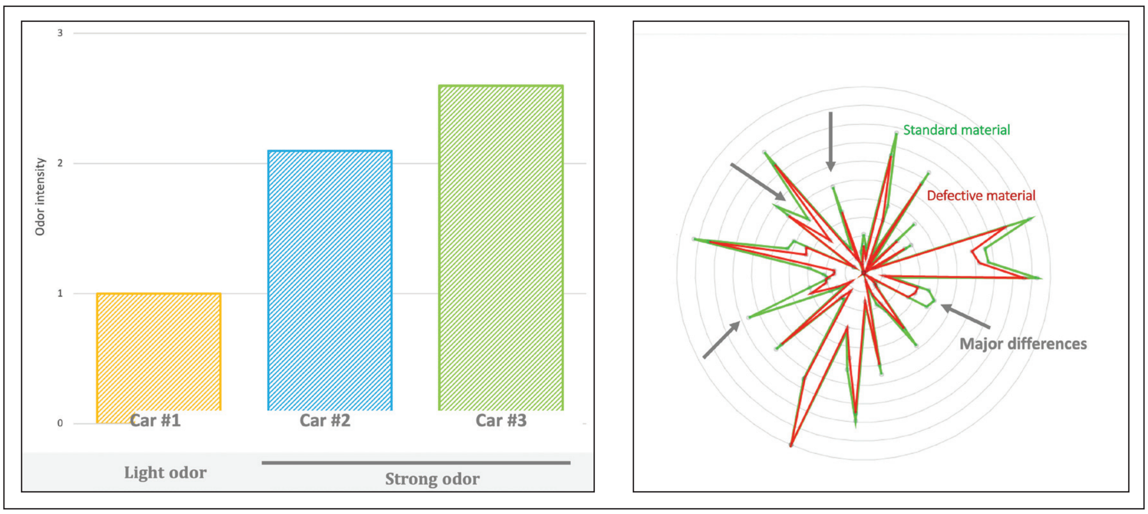

Figure 3a and 3b highlight how a ride-hailing or car-sharing company might be able to determine when a car needs to be serviced. Figure 3a clearly shows that car #3 has a much strong odor profile than car #1 and #2, indicating it's time for it to be cleaned before being put back into rotation. Figure 3b demonstrates the odor signature of standard materials versus that defective materials. If a digital olfaction sensor in a vehicle produced a defective odor signature, the indication is that there is something wrong with the vehicle.

LIGENTEC

grows portfolio and expands board to spur growth

PIC Magazine Technical Editor Mark Andrews interviewed LIGENTEC co-founder, Dr. Michael Geiselmann, about the company's latest innovations, news and recent board additions as the company expands to meet growing demand.

Michael Geiselmann

LIGENTEC, located at the EPFL (École Polytechnique Fédérale de Lausanne) Switzerland, is a foundry service provider that manufactures Photonic Integrated Circuits (PICs) for customers in high-tech areas such as datacom, quantum technologies, space, LiDAR and sensing.

As explained by company co-founder Dr. Michael Geiselmann, LIGENTEC has commercialized its all-nitride-core technology, enabling the development of products that support Industry 4.0 and other wide-ranging applications. Photonic integration is the process of downsizing optical components typically utilizing processes and techniques that have enabled microelectronic devices such as CMOS ICs to reduce their size while increasing performance. The emergence of photonic integration techniques is built around the idea of using photons instead of electrons as the basis for future advances in datacom, telecom and new photonic computing technologies. A miniaturized footprint can make optical operations much more power efficient and cost effective to manufacture.

MA: After creating a PIC component concept, that idea needs to become an actual design to be in a future MWP run – Has LIGENTEC made advances to ease the design phase?

MG: Back in March (2019), LIGENTEC streamlined the design process for SiN photonic integrated circuits (PICs) with VPI Photonics and its current partner, VLC Photonics.

Designers that use LIGENTEC AN (all-nitride) technology will now benefit from a workflow that starts from a graphical photonic integrated circuit (PIC) design and system simulation environment, which seamlessly couples to layout design tools for scripted circuit layout and DRC capabilities. The new workflow is based on LIGENTEC and VLC Photonics reference designs with the simulation software by VPIphotonics using verified measurements of fabricated chips.

The design workflow is enabled by the new VPItoolkit PDK LIGENTEC – a pluggable toolkit extension to VPIcomponentMaker Photonic Circuits; it adds support of the AN800, which is LIGENTEC'S 800 nm silicon nitride process available either through dedicated shuttle runs or Multi-Project Wafer (MPW) runs.

LIGENTEC's AN800 process provides many benefits including a very tight bending radius (< 0.005 dB for 10 turns); very low coupling losses (< 1.5 dB/facet); very low propagation losses (< 0.1 dB/cm) and very high power handling (up to 10 W tested).

VPIcomponentMaker Photonic Circuits is a professional simulation and design environment for large-scale PICs that offers a sizeable mix of general-

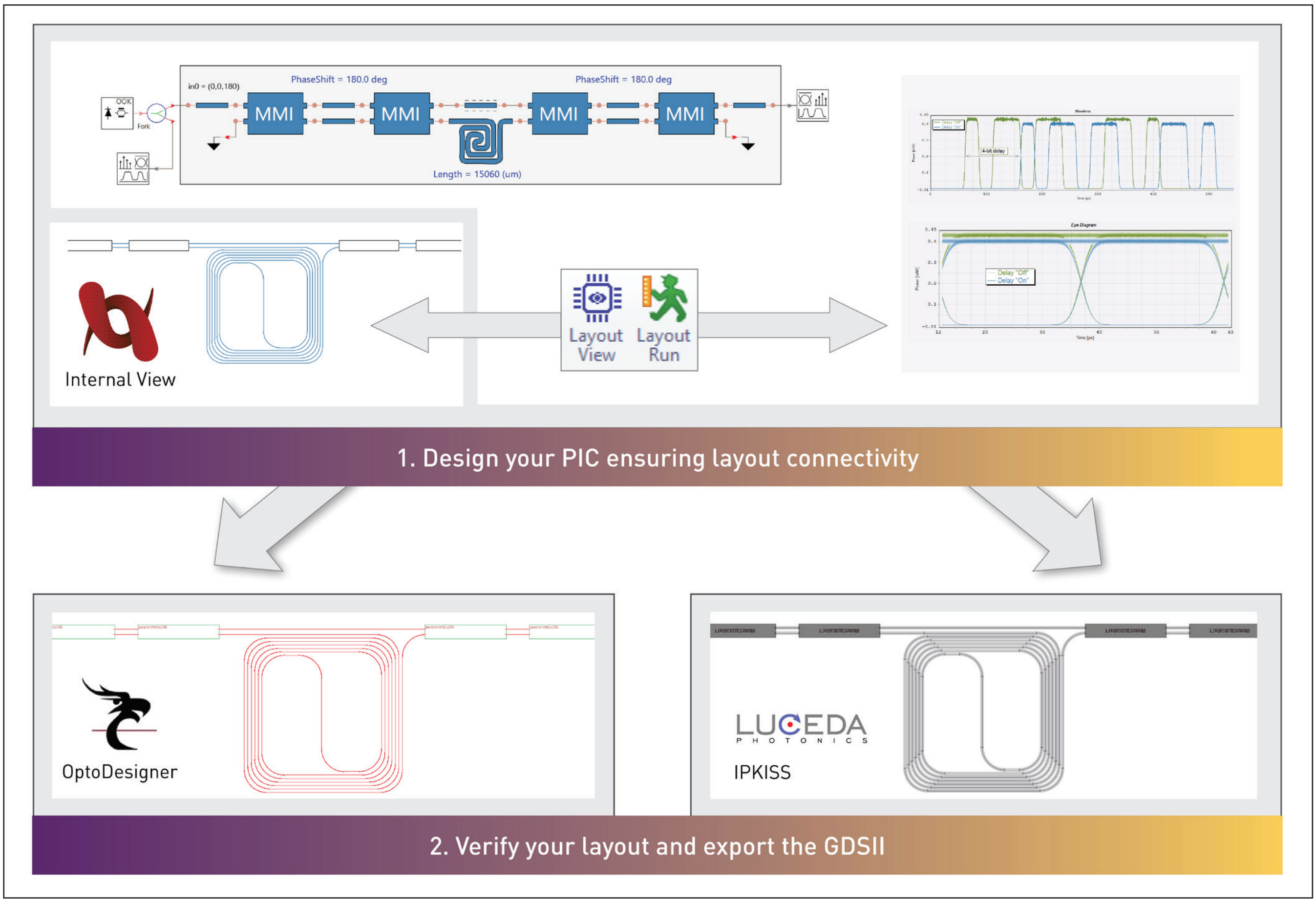

Figure 1: LIGENTEC brings your ideas to reality. Whether you are exploring new areas for your business or looking for fast prototyping at shared cost, LIGENTEC proposes their Multi Project Wafer (MPW) programme as a solution.

purpose photonic, electrical and optoelectronic device models, together with advanced circuit optimization and yield analysis capabilities. The VPItoolkit PDK LIGENTEC library extension adds foundry-certified simulation compact models for the standard building blocks supported by the AN800 process and enables a layout-aware schematic-driven PIC design workflow, including chip layout optimization according to the device's required optical functionality.

Importantly, it also allows designers to construct their own hierarchical and custom building blocks, effectively expanding the foundry PDK to fit individual needs. The layout for photonic integrated circuits designed through the process can be automatically exported to IPKISS by Luceda.

Customers gain access to LIGENTEC's mature silicon nitride photonics fabrication line, specially developed modules and optimized building blocks for design implementation. LIGENTEC allows its customers to share space on the reticle, which keeps costs down.

To employ the benefit of large transparency window of SiN, the company suggests processes adapted for near-/mid-IR and for visible wavelength range; applications targeting these wavelengths tend to benefit most from SiN technology including everything from quantum communications and LiDAR to bio-sensing and microscopy.

MA: How is LIGENTEC positioning itself to grow into its next stage of development as the movement to replace electrons with photons gathers momentum?

MG: LIGENTEC recently announced the appointment of an experienced photonics & sensors executive, Dr. Thomas Hessler, as a new member of the company's Board of Directors.

Thomas is a very valuable addition to our company in several aspects: He brings not only his knowledge of the Swiss ecosystem and his worldwide connections to key market players, but also understands the technology and its potential to open new market areas that still have to be developed.

His leadership skills and insights are to be put to good use to support the next stage of growth for LIGENTEC. Thomas takes what is considered a holistic approach to achieving success. His hands-on knowledge, built over years of experience growing a company, along with an extensive network of professionals and decision makers, is a great asset. Access to his knowledge and network will help position LIGENTEC for success.

Hessler brings over 20 years executive management experience in high-tech B2B with a focus on photonic and sensor devices. His former company, Axetris AG,

Thomas Hessler

MPW number	SiN thickness	Registration deadline	Tape-in	Expected die delivery
LGT-MPW-VIS-02	150nm	29/03/19	12/04/19	12/07/19
LGT-MPW-IR-09	800nm	31/05/19	14/06/19	13/09/19
LGT-MPW-VIS-03	150nm	26/07/19	09/08/19	08/11/19
LGT-MPW-IR-10	800nm	06/09/19	20/09/19	03/01/20

Table 1: LIGENTEC's next multi-project wafer (MPW) dates

became a market leader for micro-optics, optical gas sensing components and specialty MEMS foundry services with applications in automotive, medical, analytical and industrial spaces.

At the time of his board appointment, Hessler remarked, "LIGENTEC's groundbreaking all-nitride-core technology combines low propagation loss with small device structures; it offers the best of both worlds compared to conventional photonic integration technologies.

Its ability to be integrated easily with fibers and active functionalities will be key to achieve success in many PIC applications such as datacom, space, LiDAR and sensing. I'm excited to join the great entrepreneurial team at LIGENTEC."

MA: One f the greatest challenges facing the PIC industry is test, assembly and packaging (TAP) solutions; fiber-to-chip coupling is often considered a 'bottleneck.' Does LIGENTEC have a solution to help remedy this issue?

MG: Even though PICs become more and more sophisticated and functional, there is still an issue of non-efficient input-output interfaces, which introduce quite significant coupling-related losses. Even though academic researchers and industry insiders are pushing the limits of integrated photonics technology to improve propagation losses by hundredth of dB/cm on a chip, we are still seeing losses of up to several dB per facet! This fact greatly limits the integration of PIC technology into the existing ecosystem of optical and optoelectronic systems.

Today, the most efficient ways of communication for PICs with the "outside world" require UHNA or lensed fibers, which are non-standard (compared to the more commonly used fibers seen in today's optical systems); they are expensive and hard-to-handle.

Moreover, they are very sensitive to alignment due to the small mode field diameter. Altogether, this leads to expensive and complicated packing (or system integration) procedures, hardly compatible with the high volume requirements of telecom and datacom applications.

To overcome this obstacle, LIGENTEC developed and patented a brand new "X-Spot" module - an optical I/O interface with large mode field diameter matching that of the SMF-28 fiber. It allows unprecedented coupling efficiency (<1dB) for thick film PICs with industry standard optical fibers and significantly decreases the price and efforts for packaging procedures.

"Having a mature, ultra-low-loss platform with highly efficient fiber-to-PIC communication brings us one step closer to achieving the bright future of integrated photonics," Geiselmann concluded.

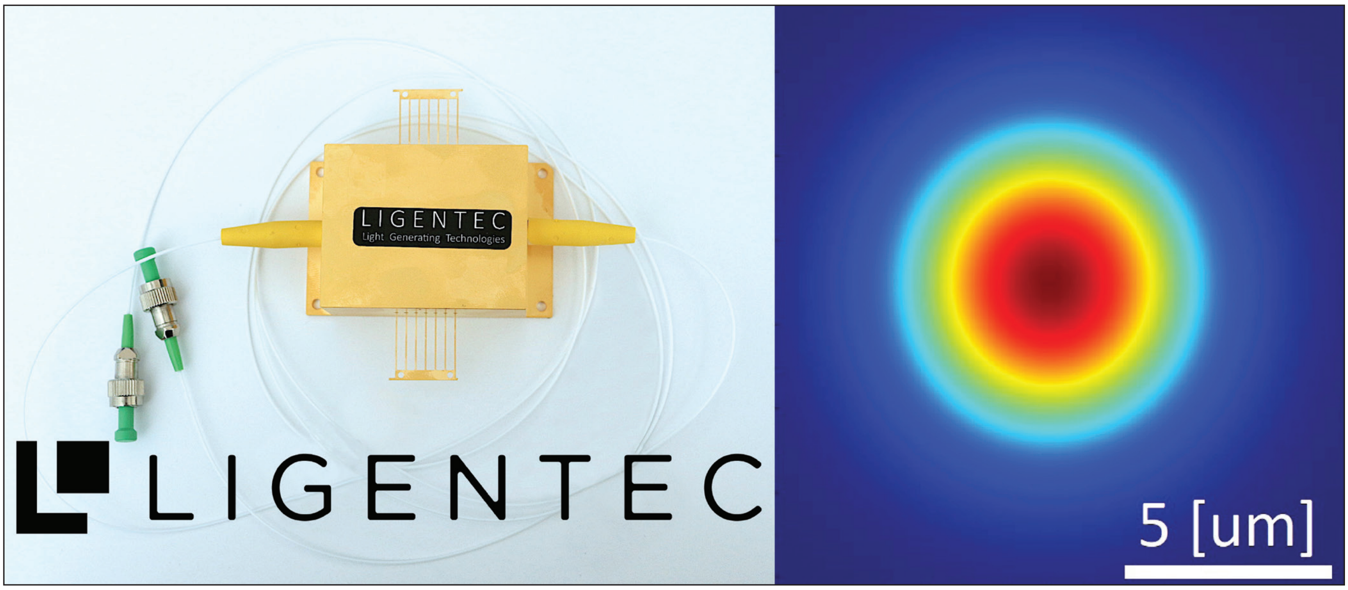

Figure 2: LIGENTEC developed and patented its new "X-Spot" module - an optical I/O interface with a large mode field diameter that matches SMF-28 fiber; this advancement can dramatically reduce coupling-related signal losses.

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Size and performance

advantages create new indium phosphide MZM opportunities

Fraunhofer HHI experts explain how long-haul telecom and datacenter applications can benefit from new generations of Indium phosphide MZMs to satisfy challenging bandwidth, size and power consumption requirements.

By Gerrit Fiol, Karl-Otto Velthaus, Marko Gruner, and Klemens Janiak, Fraunhofer Heinrich-Hertz-Institute

THE EVER-GROWING NEED for more bandwidth, miniaturization and reduced power consumption has driven the commercialization of Indium phosphide (InP) Mach-Zehnder modulators. Originally meant for long-haul communications, new developments are making them attractive for metro or even short reach communication, e.g. inside a datacentre.

We believe that emerging silicon photonics (SiP) technologies are an excellent candidate for the 3 cm to 30 cm reach due to the mature silicon integration technology; however, for all other remaining applications, InP is the better choice.
The InP MZM offers a high electro-optic phase shift capability through the incorporation of Multi-Quantum-Well (MQW) active media and resulting Quantum-Confined-Stark-Effect (QSCE) [1]. This leads to a very small half-wave switching voltage ($V\pi$) in the order of 0.5 V cm, which is directly linked to the power consumption of a transmitter. The employed concept of a capacitive loaded traveling-wave electrode (CL TWE) enables high electro-optic (eo) bandwidth without compromising $V\pi$ [2].

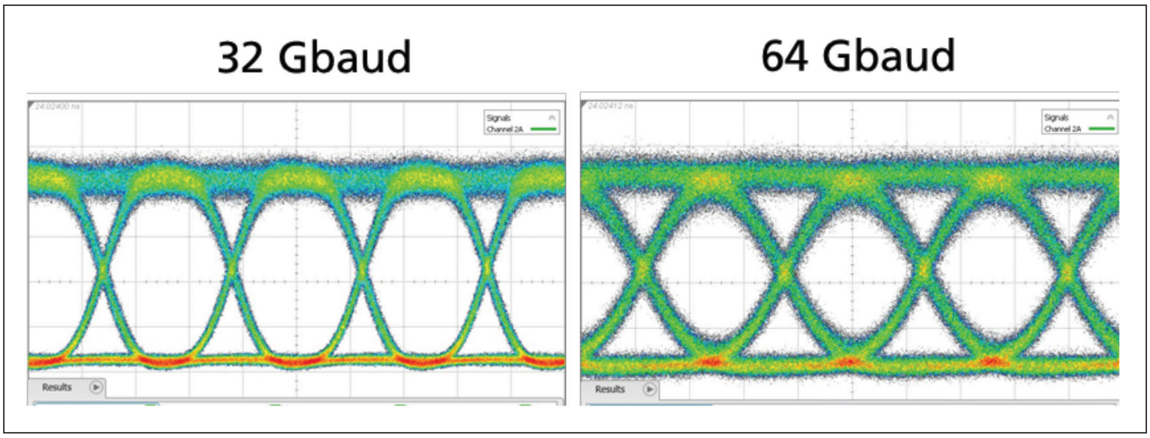

Figure 1: DFB laser integrated MZM at 1300 nm for two different Baudrates

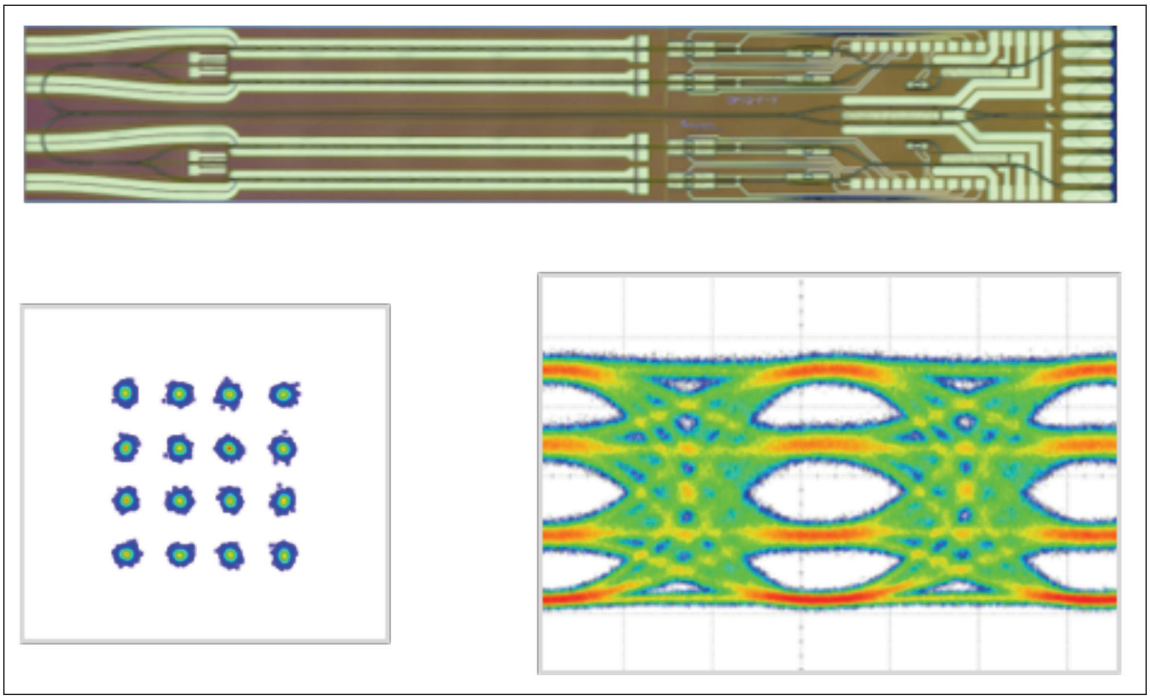

Figure 2: Dual IQ-Modulator with integrated pre- and post-SOA (top), bottom left: 32 Gbaud PAM optical eye diagram from one MZM, bottom right: 32 Gbaud 16QAM constellation diagram of one IQM

The industrial demand on these photonic integrated circuits (PICs) focuses on the following topics:

- Active media integration (laser/semiconductor optical amplifier)
- Scalability
- Electronic co-design
- High-baud rate capability
- Uncooled operation
- Full C-/ or O-Band wavelength coverage
- Ultra-low drive voltages

Mach-zehnder modulators for long reach

One of the main advantages of InP, compared to silicon, is the possibility to incorporate active devices like lasers or semiconductor optical amplifiers (SOA), which has been successfully developed at HHI and already transferred to commercial applications.

Laser and SOA integration is commonly presented for wavelengths within the C-Band. With the application of MZMs for rather short distances, down to a few km or less, an operation within the O-Band is of interest and sometimes advantageous. It enables transmission with dispersion values close to zero.

This simplifies receiver post-processing and saves power consumption in case of coherent detection. The InP material system offers the possibility to shift gain elements as well as all other functional elements to the O-Band operational window by re-designing the semiconductor layer stack and their respective waveguide dimensions accordingly.

All high-frequency properties as already obtained for C-Band operation can be transferred. Depicted in Figure 1 are the eye-diagrams for 32/64 Gbaud operation at 1300 nm.

To enable scalability e.g. arrays of MZMs, the two major considerations are RF-feed and RF-termination as well as optical coupling. A design where the RF is fed from one side and the optical coupling from the other is a viable approach. An example of such a device is the Dual-IQ modulator (IQM) depicted in Figure 2, with the RF lines entering from the left side and all optical ports being on the right side.

RF-termination is integrated on chip. It also comprises pre- and post-SOAs to achieve a virtually zero insertion loss (IL) device and to equalize the optical power in the two IQMs. Each IQM is designed for

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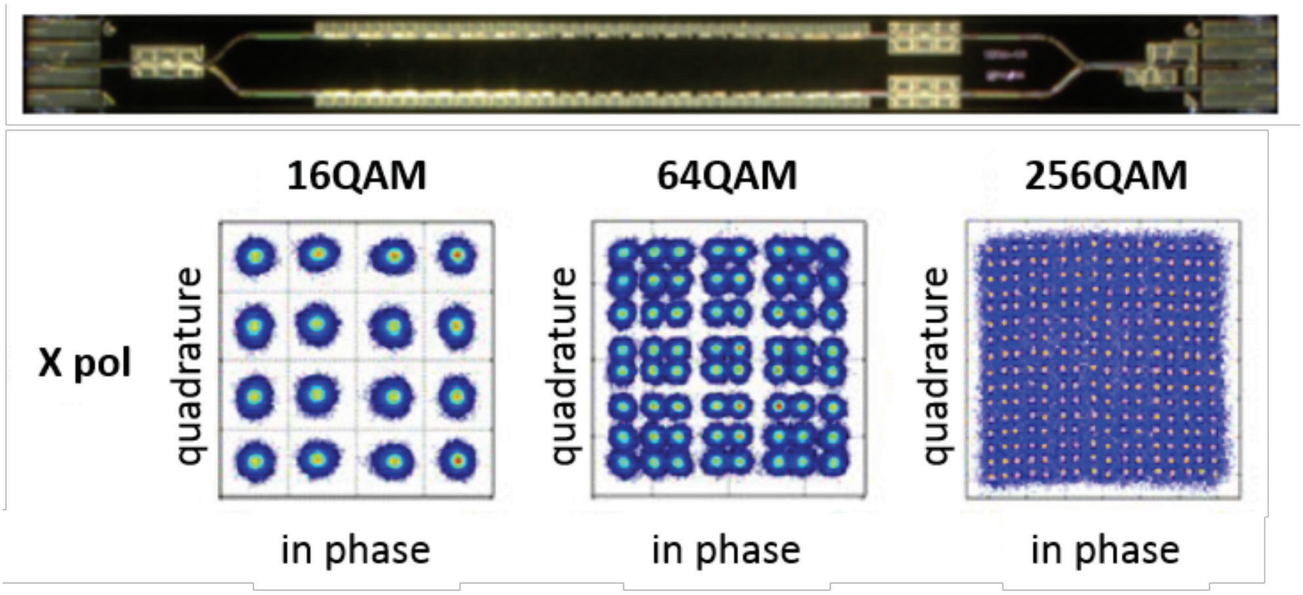

Figure 3: Segmented InP IQ Modulator (top) and received constellation diagrams at 32 Gbaud and 16QAM, 64QAM as well as 256QAM

and operated at 32 Gbaud using 16QAM enabling 256 Gbit/s using two polarization. [3]. The co-design of driver and MZM has become attractive due to the possibility of realizing more advanced configurations (e.g. segmented MZM [5], [6]) or impedance engineering for improved power consumption. Therefore, Fraunhofer HHI has added this co-design ability to its portfolio.

Segmented MZM´s behave as a direct electrical to optical DAC and therefore offers an operation without the use of power hungry digital-to-analogue-converters (DAC) [6]. Due to the absence of the TWE the segments are connected to a customized driver, enabling the afore mentioned DAC-less operation and/or linearization features. Results obtained at 32 Gbaud with up to 256QAM are shown in Figure 3. [4]

The hybrid co-design and co-integration of driver and MZM offers the chance to take the best material of both worlds. Combining the best driver with the best modulator results in lowest power consumption at highest performance. An example is given in Figure 4, showing a DFB laser integrated IQM with Co-designed driver. [8], [9]. The overall power consumption of driver and IQM is only 1.1 W.

Mach-zehnder modulators for short reach

Recent developments, discussions and standardization within photonics-based data and telecom applications are all targeting high modulation rates with 100 Gbaud and beyond in the near future. The InP MZM is a well suited eo-modulator for such kind of speeds with its unprecedented combination of high bandwidth, low $V\pi$ and low optical (chip) loss. In terms of power consumption an uncooled operation is desirable, leading to athermal operation of the MZM.

The high-speed modulators are based on the above-described CL-TWE concept. Due to their design, they can be operated in a 50 Ohm single ended or 2 x 25 Ohm differential configuration. The

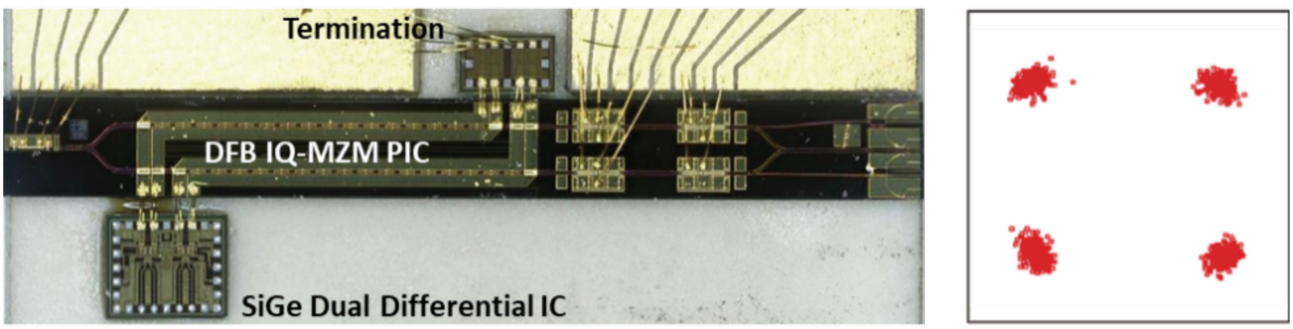

Figure 4: DFB laser integrated IQM with Co-designed dual differential driver and external termination (left), right shows the 32 Gbaud QPSK constellation diagram. The device is operated at 1550 nm.

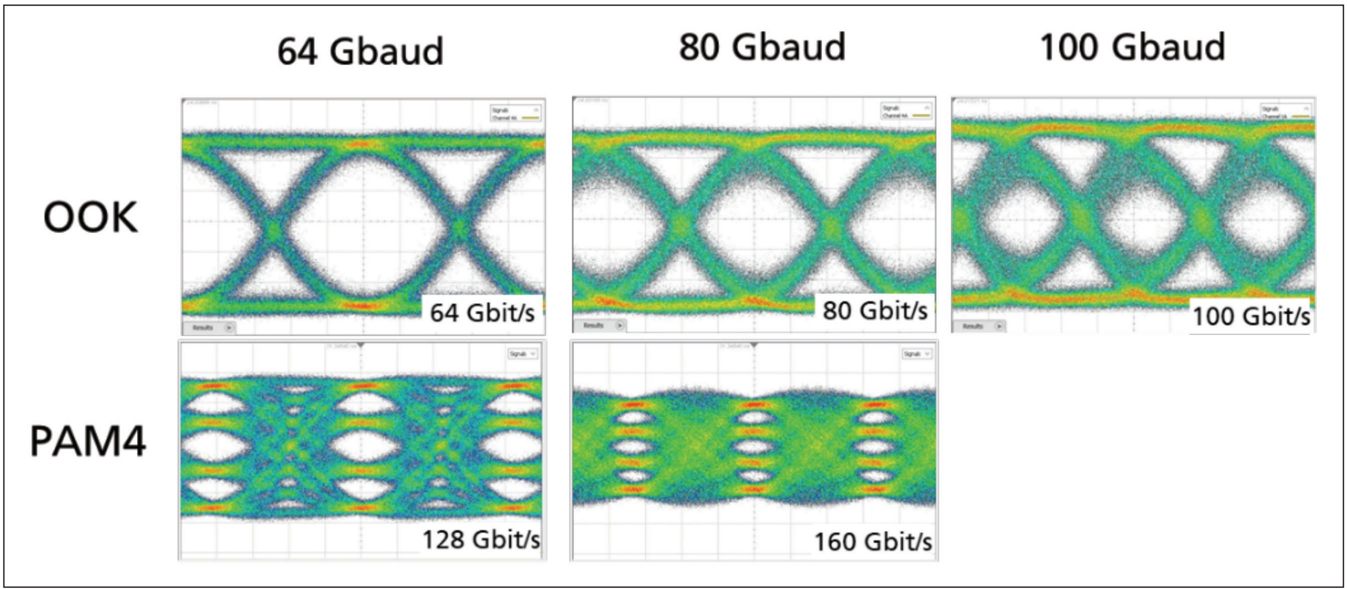

Figure 5: Optical eye diagrams generated with an MZM at a wavelength of 1550 nm, top row shows the one for OOK modulation while the bottom shows PAM-4 modulation. Baud rate increases left to right from 64 Gbaud to 80 Gbaud and 100 Gbaud

two waveguides of the interferometer are acting as two capacitive loads connected in series. This enables intrinsic push-pull configuration leading to a non-chirped optical signal, preferred for optical communication.

The use of a TWE enables velocity matching between electrical and optical wave through the capacitive loading effect. The resulting smooth roll-off of the electro-optical transfer function allows for modulation rates beyond the 3-dB electro-optical bandwidth. The MZM is operated from 64 to 100 Gbaud. Dynamic extinction ratio (ER) for 64 and 80 Gbaud are >10 dB and drops to 8 dB for 100 Gbaud. While the OOK eye diagrams are generated using a bit pattern generator, an arbitrary waveform generator (AWG) with pre-equalization is used to generate the PAM-4 shown in Figure 5.

The MZM is operated across the entire C-band with temperatures ranging from 15°C to 85°C (thermo-electric cooler temperature) at 64 Gbaud using NRZ OOK. The results are plotted in Figure 6. The dynamic ER is ~10 dB. When the temperature is changed the backplane bias has to be adjusted accordingly. Adjusting the backplane DC-bias of the MZM allows for efficient control of $V\pi$ (respectively ER) and subsequently controlling the dynamic performance

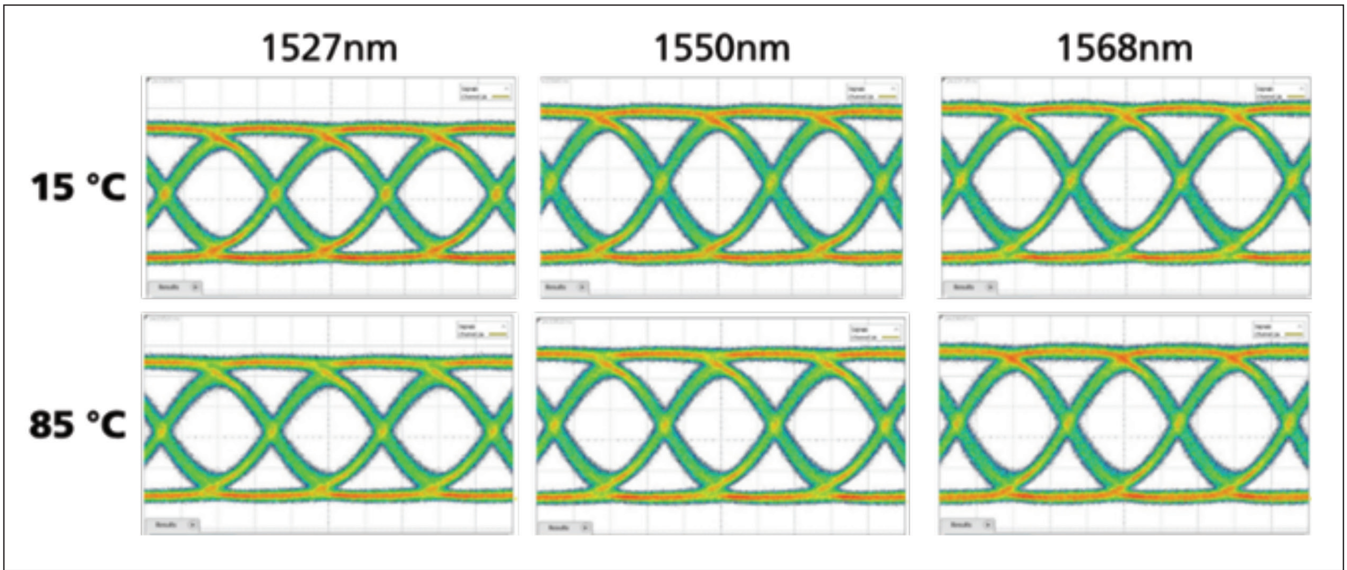

Figure 6: Optical eye diagrams generated with an MZM at 64 Gbaud OOK modulation, the TEC temperature is set to 15°C (top row) or 85°C (bottom row). The laser wavelength was set to 1527 nm, 1550 nm and 1568 nm (left to right)

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We will dive into the growth in edge networking devices and network protocols (such as OPC UA and MQTT) and ways these are evolving to enable completely new analytical capabilities. We will also explore how sensing devices as well as analytical/AI software can be rethought to help manufacturers utilize their data for improved profitability and market reach.

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We will explore the complementary roles of sensor fusion and data fusion as a means to integrate multiple data sources to produce more consistent, accurate, and useful information than is possible using a single data source. We will further explore the variety of key sensor fusion algorithms available to designers including those most commonly used across today's markets in consumer and commercial applications.

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We will explore the challenges of manufacturing sensors that withstand harsh environmental conditions along with key issues tied to powering devices and securely collecting data from sensors deployed in harsh environments. We will also explore the expanding need for sensors and sensor fusion approaches specifically for use in harsh environments as well as the special challenges in designing for space, aviation and aerospace applications.

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We will delve into how simulation and automation providers are integrating new sensors and SoCs into testbeds for enhanced performance and illustrate how sensor and data fusion, machine learning and AI can enhance simulator performance while extending the benefits of automation into nondigitized sectors.

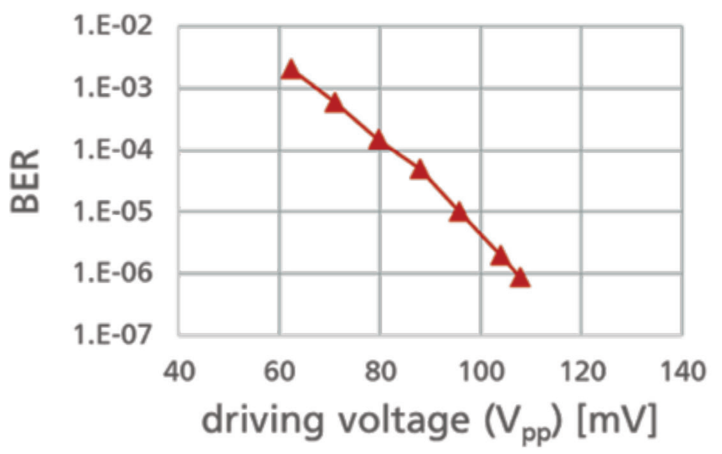

Figure 7: Bit Error ratios for an MZM operated at ultra low drive voltages. Modulation rate is 64 Gbaud and modulation format OOK at a wavelength of 1550 nm.

of the MZM. The backplane bias never exceeds the 2-8 V range for all temperature/wavelength combinations. The moderate backplane bias ensures that the voltage dependent optical loss is not limiting the performance with increasing bias. This is a very easy and comfortable way to realize an athermal operation across the entire C-band.

Mach-Zehnder Modulators at ultra-low power Multistage analogue amplifiers, integrated together with the MZM into a transmitter/transceiver module, commonly drive the MZMs. Typically the output voltage swing required is larger than 1 V with the power consumption being directly linked to the squared voltage. The realization of error free optical transmission with drive amplitudes lower than 1 V or even lower to circumvent the use of a driver improves the power consumption of the optical transmitter. The drive amplitude can be much smaller than the $V\pi$ of the modulator.

In Figure 7 the drive amplitudes are between 3% and 6% of $V\pi$. We have operated the modulator at a TEC temperature set to 40°C. The 64 Gbaud PRBS 15 signal is directly fed from the bit pattern generator into the MZM. BERs are retrieved by using a real time oscilloscope and offline processing including clock recovery, resampling and equalization.

Figure 7 shows the BER vs. drive amplitude with a BER for 60 mV which is still below the 7% OH HD-FEC of 3.8 10^{-3} [7]. Such small drive amplitudes enable driver-free operation and are fully CMOS compatible. These drive amplitudes result in 0.6 fJ/bit. Yet further improvement is possible by optimization of power consumption, effort and error correction.

Conclusion

InP technology enables 15-85°C operation of full C-band 100 Gbaud MZMs. Active media integration, such as lasers or SOAs, as well as scalable layouts greatly improve PIC versatility and broadens the field of application. The electronic Co-Design offers high speed operation at lowest power consumption.

The power consumption can be further reduced when driving the MZM with amplitudes as low as 60 mVpp. All these features enable InP based MZMs to be a highly versatile and highly efficient eo-modulator for long as well as short reach-communication.

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Applications of integrated poly-si LEDs as on-chip micro biosensors

The authors describe ways that monolithically integrated light-emitting devices (LEDs) can be utilized in new sensing systems where their precision and high performance can enhance bio-sensing techniques for healthcare and wellness.

By co-authors: Guanhua Huang[a], Kaikai Xu[a*], Jianming Zhao[a], Lukas W. Snyman[b] and Herzal Aharoni[c]

SILICON plays an irreplaceable role in electronic industry, while it was previously rarely seen in photonics applications. Silicon has abundant reserves on the earth, which has contributed to its widespread use and continuing research. Silicon-based devices are the most suitable materials for integrated processing functions so far because of decades of development around this material and researchers' countless efforts. However, because bulk silicon is an indirect bandgap material with low luminescence efficiency, it has previously been considered a poor optoelectronic material. But with further study of silicon materials, new characteristics including silicon-based luminescence have been found. What's more, because of silicon's mature fabrication technology, low cost, and CMOS compatibility, the development of silicon photonics is welcomed by photonic and electronic manufacturers.

Optical-electronic integrated circuit technology is becoming one of the most important spotlights in the past decade, for its paramount advantages, such as low-power, anti-interference, etc. Therefore, more and more attention has been paid to the research of Si-based luminescent materials in recent years. Since Newman revealed the physical phenomena that silicon PN junctions can emit light in reverse bias, some researchers have studied the light luminescence mechanism in different *p-n* structures of silicon quite intensively. At present, there are various methods for realizing silicon-based luminescence, such as porous silicon luminescence, Er-doped silicon luminescence, super lattice quantum well structure, etc. However, these methods have not been widely used so far, mainly because of their materials or device structures that could not meet the requirements of today's optoelectronic monolithic integration for the process

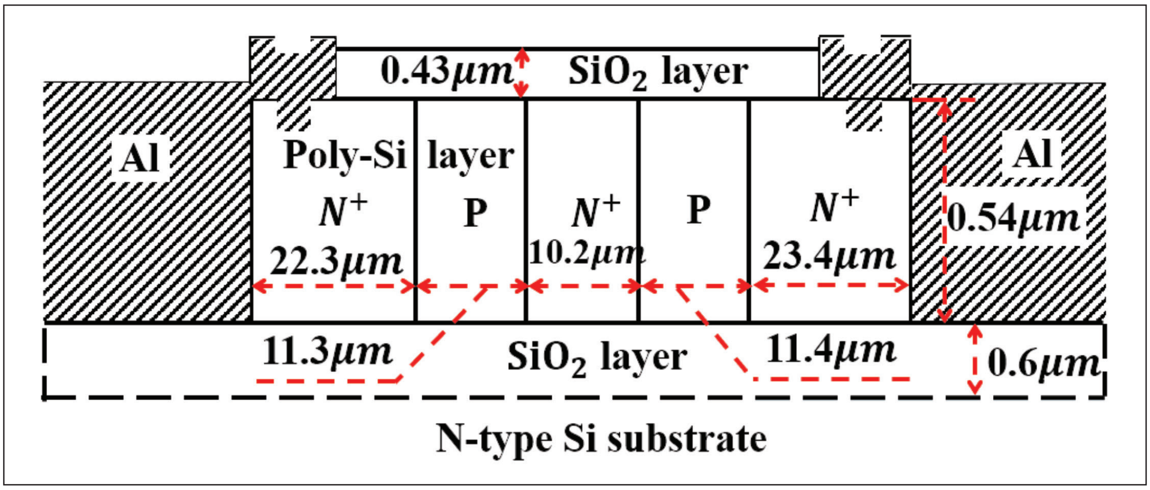

Fig. 1: Schematic cross sectional view of the proposed device

and luminous efficiency of light-emitting devices. Therefore, the main difficulty in the current all-silicon optoelectronic integration is how to be compatible with the standard Si-CMOS processing technology.

Kaikai Xu's research team recently had realized a compact poly-silicon light emitting device that is compatible with standard VLSI processing. For the base of poly-silicon layer, this new type of light-emitting device can be fabricated with traditional standard CMOS technology. This silicon light source could find some applications in on-chip optical interconnections and in electro-optical conversions in future all-silicon integrated photonic circuitry. There is also a prospect for on-chip electro-optical conversions in future all-silicon integrated photonic circuit.

Shown in Fig.1, this current-controlled two-terminal device's N+-P-N+-P-N+ regions based conduction channel is created on the SiO_2 layer which is quite similar to two reverse bias p-n junctions and two forward bias p-n junctions connected in series. The reverse-biased PN junctions serve as photon generation sources, and operate with other two forward-biased p-n junctions to favor various direct and indirect inter-band transitions in silicon, thus realizing hot carrier luminescence in silicon devices.

The poly-silicon LED mainly had four layers. We can learn the main structure of this LED from Fig. 1 and Fig. 2. The first layer is the n-type Si wafer as the substrate. The second layer, a SiO_2 layer is deposited on the wafer. This layer is utilized to reduce the basal-plane stacking fault density and to reduce the isolation current from the bulk silicon, just like most CMOS manufacturing process. Then the poly-silicon layer is deposited on the first SiO_2 layer. After that, mask layer is used to limit the dopants implantation, so the *n+-p-n+-p-n+* structures can be formed in the poly-silicon layer. After depositing another protective SiO_2 layer, aluminum is deposited at both sides of this device as electrodes of the LED.

The dominant role of non-radiative recombination at the N+ and P+ contacts is diminished by confining the injected carriers around the PN junction's interface in which avalanche takes place. The optical emission from the device is concentrated in the avalanche region, and hot carriers are generated during the avalanche process, which makes the current-related radiation present a broad band in the range of 400-900 nm. There is no obvious shift of the spectrum with different driving voltage.

Fig. 3 shows the electroluminescence spectrum of the visible light as emitted from the device. The graph shows that the electroluminescence spectrum has a broad emitting wavelength range from 450 nm to 890 nm. The peak at 680 nm may relate to indirect radiative recombination between the conduction band and valence band. Through experimental assistance and numerical calculation for the emission efficiency,

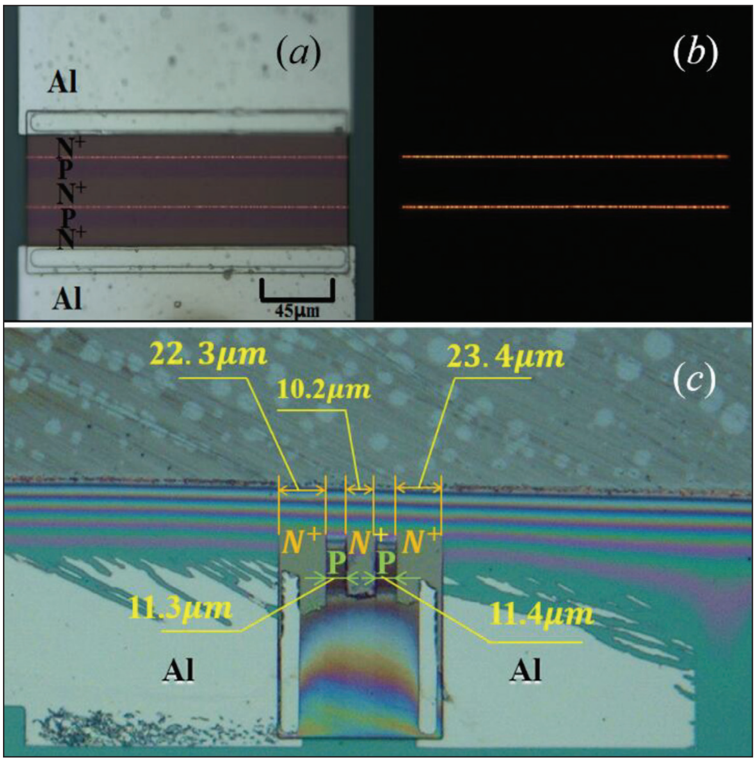

Fig. 2: (a) Bright field microphotograph of poly-LED; (b) Dark field micro-photograph of poly-LED; (c) The cross section of the dyed poly-LED.

it is obtained that the external quantum efficiency (QE) is of the order of 10−7, presenting higher emission efficiency, using carrier-injection engineering with revised bipolar-junction device structure, shown in Fig. 4.

In this feature, *n+pn+pn+* device structure is proposed to increase the efficiency of a silicon (Si) avalanche mode light-emitting diodes (AMLEDs) [1]-[2]. This structure comprises two reverse-biased

Professor Xu's students are measuring Poly-Si LEDs for future potential applications of On-Chip Micro Biosensors (on the right side, Guanhua Huang, with his partners)

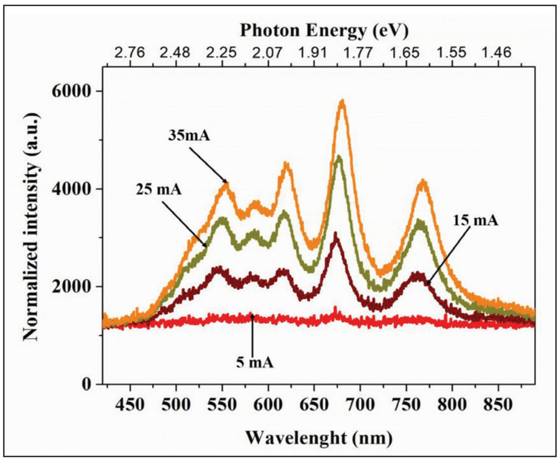

Fig. 3: Normalized field emission spectrum from reserve-bias junctions at room temperature in different drive current.

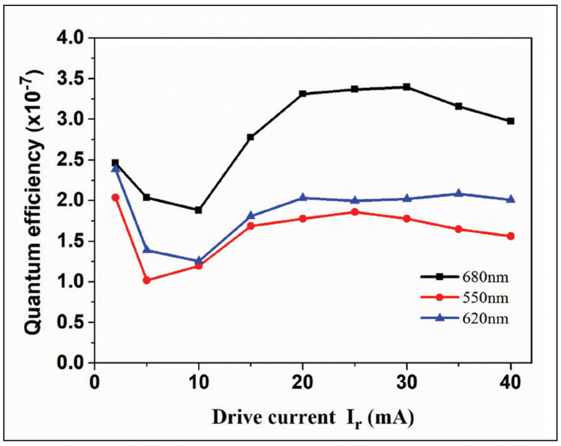

Fig. 4: Relationship between the drive current and the external quantum efficiency (QE), electric-optic power conversion efficiency(PE).

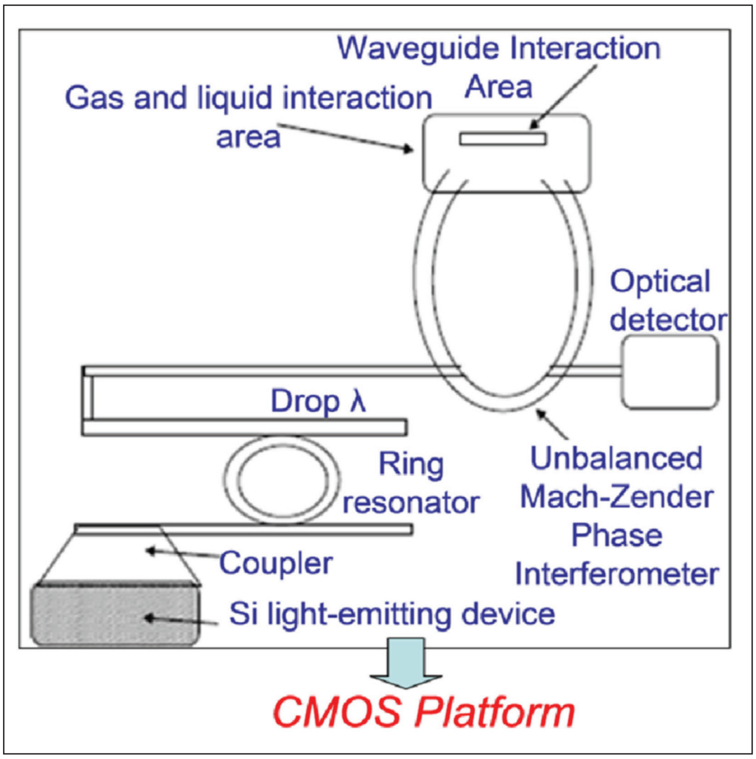

Fig. 5: Schematic diagram of a CMOS-based micro-photonic system that can be realized using an on-chip Si light-emitting device, a series of waveguides, ring resonators, and an unbalanced Mach-Zehnder interferometer.

light-emitting junctions and two forward-biased junctions to increase intraband transitions by providing extra carriers. Such a device structure could also improve the speed. A hypothetical micro-photonic system is demonstrated in Fig. 5 consisting of a silicon light-emitting device, and a silicon-based detector together with waveguides integrated monolithically in a CMOS structure. Wide area silicon light-emitting devices are used in order to increase the total optical emission power into the waveguide. Near the layout end, an opening is integrated in the CMOS over layers by post processed RF etching to enable gas or liquids to interact with the evanescent field of a waveguide section and introduces intensity and/or phase contrast changes.

Conclusion

We have demonstrated that a complete micro-photonic sensor system can be integrated into standard CMOS circuitry. A section of the waveguide shown in Fig. 5 is exposed to the environment and can detect phase and intensity contrast due to absorption of molecules and gases in the evanescent field of the waveguide. The optical source & photo-detector and waveguide arrays can be arranged to act as high performance sensors in emerging fields like bio-sensing and nanotechnology [4].

Reference

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For more information about the device, please check the following articles:

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